1568
doi:10.1017/S1431927616008680

Microsc. Microanal. 22 (Suppl 3), 2016
© Microscopy Society of America 2016

Nanocharacterization of Strontium Titanate Thin Films and Oxide-Electrode Interfaces in Resistive Switching Devices

William J. Bowman[1,2], Eva Sediva[2], Peter Crozier[1], Jennifer L.M. Rupp[2]

[1.] School for the Engineering of Matter, Transport and Energy, Arizona State University
[2.] Electrochemical Materials Group, ETH Zürich, Zürich, Switzerland

Thin film resistive switching devices based on perovskite $SrTiO_3$ (STO) are the subject of recent studies focused on defect kinetics [1] and electrochemical switching mechanisms [2]—work which has addressed critical aspects of material performance and device design [3]. However, nano- and atomic-scale understanding of switching mechanisms, and the role of device fabrication parameters on switching behavior and device performance is an ongoing area of research [2]. Further, multi-bit architectures offer higher device density, so guidelines for design, fabrication and characterization of these devices is desired. We investigate nano- and atomic-scale aspects of single- and stacked multi-bit thin film resistive switching devices with varying electrode materials and thin film stacking schemes. From a materials perspective, we focus on oxide microstructure, potential highly defective zones, and their interfaces with the different electrodes employed.

We have fabricated a series of resistive switching devices (see figs.1b and 2a) based on STO thin films using pulsed laser deposition (PLD). Our devices show a stable resistive switching behavior in their I-V characteristics. The influence of electrode materials, substrate adhesion layers and STO microstructure is under investigation. Furthermore stacked devices of multiple single bits are fabricated and characterized in terms of single and multi-bit switching. For example, in the Pt|STO|Pt resistive switching device shown in fig. 1, the morphology of the top and bottom Pt electrodes varies considerably (this effect is also clearly observed in the device shown in fig. 2a). During STO growth the substrate and bottom Pt electrode are heated to 650 °C, which allows the Pt (deposited at room temperature by electron-beam evaporation) to anneal and produce a rather smooth interface with the columnar grained STO, fig. 1a. From Fourier analysis of atomic-resolution images, oriented growth of STO (Pm-3m) on Pt (Fm-3m) was observed in the 111 growth direction (i.e. vertically in fig. 1a). Conversely, the top Pt electrode is deposited following the growth of STO, which exhibited approximately 20 nm surface roughness, resulting in porous, granular Pt with a tortuous STO-electrode interface, fig. 1c. Images of the top Pt-STO interface revealed a diffuse interfacial region between Pt crystals comprising the metal electrode, and crystalline columnar grains of the STO film. In a second switching device with a Ti metal adhesion layer deposited between sapphire substrate and bottom Pt electrode (fig. 2), STEM ADF and EDX elemental mapping has been performed to investigate the compositional distribution throughout the device. Again dissimilar electrode morphologies were observed: Dense Pt below the STO formed a mostly smooth and well-defined oxide-electrode interface, and more porous granular Pt above the STO formed a tortuous oxide-electrode interface. EDX mapping revealed that the Ti adhesion layer was not fully continuous, and appeared to diffuse through the bottom electrode to form TiO_x at the bottom oxide-electrode interface (fig. 2b,d). This interpretation is consistent with [4], and corroborated by Sr elemental map of the same region (fig. 2c), which shows the absence of Sr at the bottom oxide-electrode interface coincident with the Ti-enriched region in fig. 2b.

In this work we examine the influence of film morphology, interfacial atomic structure, composition, and chemistry at STO-electrode interfaces on the resistive switching behavior in PLD thin film resistive switching devices. We discuss device electrical behavior in light of electrode material choice (i.e. metal or oxide), and film growth strategies such as the use of adhesion layers between device and substrate.

https://doi.org/10.1017/S1431927616008680 Published online by Cambridge University Press

High resolution images and spatially-resolved spectroscopic data (i.e. EDX and electron energy-loss spectroscopy) acquired at STO-electrode interfaces are presented, with the goal of elucidating resistive switching behavior of devices. Multi-bit thin film device architectures are also currently under investigation, and device performance will be discussed in terms of nanostructures and elemental mapping. [4]

References:

[1] F. Messerschmitt, M. Kubicek, S. Schweiger, J.L.M. Rupp, Adv. Func. Mat. **24** (2014), 7448.
[2] M. Kubicek, R. Schmitt, F. Messerschmitt, J.L.M. Rupp, ACS Nano **9** (2015), 10737.
[3] R. Muenstermann, T. Menke, R. Dittmann, R. Waser, Adv. Mat. **22** (2010), 4819.4. J.J. Yang, 4. J.P. Strachan, Q. Xia, D.A.A. Ohlberg, *et al.*, Adv. Mat. **22** (2010), 4034.
[4]We acknowledge ScopeM at ETH Zürich, and thank the staff for their support. This work was supported by the Swiss NSF (project 155986). W.J.B. was a Swiss Government Excellence Scholarship holder for the academic year 2015-2016 (ESKAS 2015.1183); and acknowledges financial support of the US NSF Graduate Research Fellowship Program (DGE-1311230).

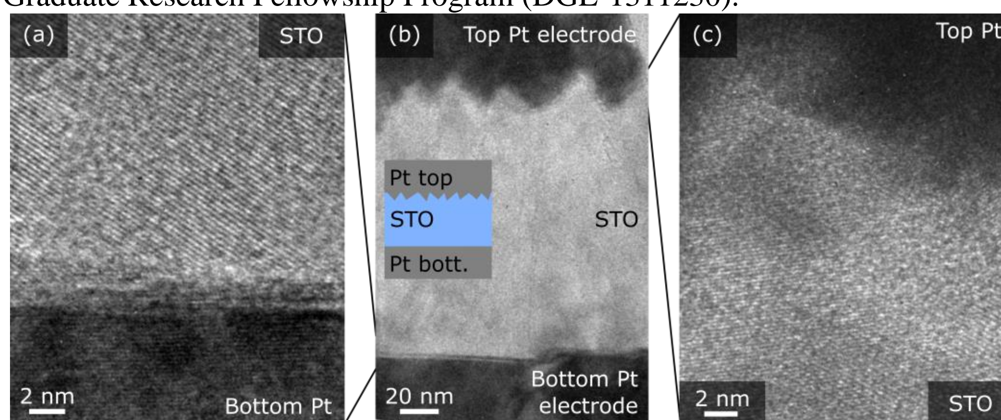

Figure 1. (a) Bright-field TEM of interface between bottom Pt metal electrode and STO thin film in the Pt|STO|Pt resistive switching device shown in (b). (b) STO film and STO-electrode interfaces in Pt|STO|Pt resistive switching device (diagram is inset). (c) Top Pt electrode STO interface. Regions shown in (a) and (c) are indicated via lines to (b). FEI Tecnai F30, 300 kV.

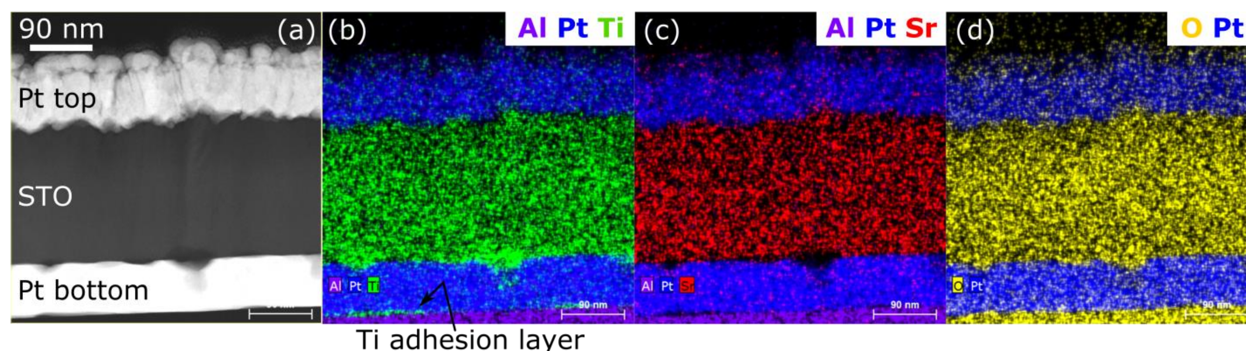

Figure 2. (a) STEM ADF image of Ti|Pt|STO|Pt resistive switching device grown on Al_2O_3. (b-d) EDX composition maps of the region shown in (a); Ti adhesion layer is highlighted in (b). Al $K_{\alpha1}$, Pt $M_{\alpha1}$, Ti $K_{\alpha1}$, Sr $K_{\alpha1}$ and O $K_{\alpha1}$ X-ray lines used; FEI Talos F200X, 4-segment EDX .

https://doi.org/10.1017/S1431927616008680 Published online by Cambridge University Press