A large silicon detector array and real-time elemental image projection of X-ray microprobe fluorescence data using pipelined, parallel processing

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The aim of this project is to integrate a large solid-angle detector array and a high speed pipelined parallel processing engine, with an embedded implementation of the *Dynamic Analysis* (DA) method for fluorescence spectra deconvolution and image projection, to yield a detection system capable of overlap-resolved real-time elemental imaging at up to $\sim 10^7$ events per second.

The detector array comprises a 384 element low-leakage Si pad array (Fig. 1) under development at BNL [1,2], with integrated low-noise preamplifier, a high order shaper with baseline stabilizer, multiplexed 12 bit ADC and over-threshold TDC to enable pile-up detection and rejection. The array is wire-bonded to 12 signal processing chips, which are water cooled with additional Peltier cooling of the detector array to -35 °C. A prototype of the detector array has recently demonstrated an energy resolution of 184 eV (Mn K_α) [3] (Fig. 2).

The DA method builds a matrix transform to perform the task of spectral deconvolution of overlapping element spectra, including fluorescence lines and detector artefacts, such as tailing and escape peaks [4]. The method was originally developed at the CSIRO to project quantitative elemental images derived from proton induced X-ray emission (PIXE) data and has been recently extended to handle Synchrotron X-ray Fluorescence (SXRF) data [5]. The DA approach lends itself to real-time processing of detected X-ray counts on an event-by-event basis. Each event is tagged by detector number and current XY position of the sample stage for imaging (and potentially E and θ for spectroscopy and tomography). The detector number is used to select DA terms appropriate to the take-off geometry of the detector element, and these terms are accumulated into the pixel selected by the associated XY tag. This close coupling of scan coordinates with data acquisition removes the common constraint of ~second dwell time per pixel, enabling high definition images to be collected. Image sizes of 500 x 500 pixels or more at dwells down to 1 ms or less are envisaged.

The parallel processing engine has been developed at the CSIRO for machine vision applications and consists of a wide input data interface, 150 MHz FPGA connected to 3 large static RAMs, Motorola PowerPC co-processor, and ample fast serial (8 x 11.1Gb/s) and Ethernet ports (2 x 1Gb/s, 1 x 100Mb/s). Code for the FPGA is developed using an in-house pipelined, parallel processing compiler called 3PL, and will handle pile-up rejection, energy calibration mapping and DA projection. The PowerPC will handle image accumulation and display and external control requests as an EPICS control node. A 155 bit I/O card will reside near the detector array and interface to the parallel processing card, located outside the hutch, via a high-speed fibre-optic link; the detector and I/O card will occupy minimal end-station real-estate.

Our goal is to have this detector system adopted for high performance imaging at the NSLS and on the Microspectroscopy beam-line (BL9) of the Australian Synchrotron [6].
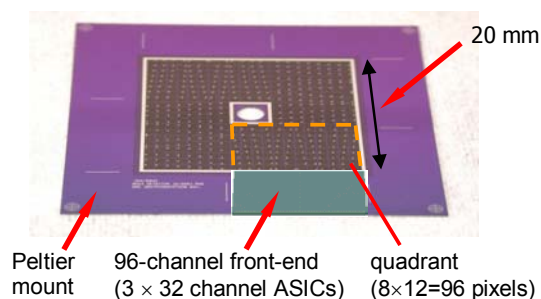
Peltier mount — 96-channel front-end (3 × 32 channel ASICs) — quadrant (8×12=96 pixels)

Fig. 1   384 element low-leakage Si pad array (each 1x1 mm^2, 250 μm active thickness, cooled to -35 °C by Peltier devices), arranged in an annular array (20 x 20 mm^2 with central 3 mm hole) for placement around the beam, and front-end signal processing ASICs arranged in 4 banks of 96 channels [1,2].
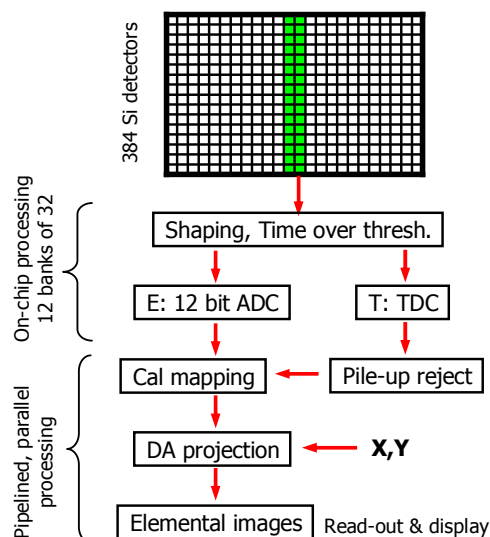

Fig. 2   Schematic illustrating on-chip processing (32 channels multiplexed into an ADC for energy and TDC for time over threshold) and pipelined, parallel processing for pile-up rejection and *Dynamic Analysis* image projection [4], using current XY stage position to select pixel.
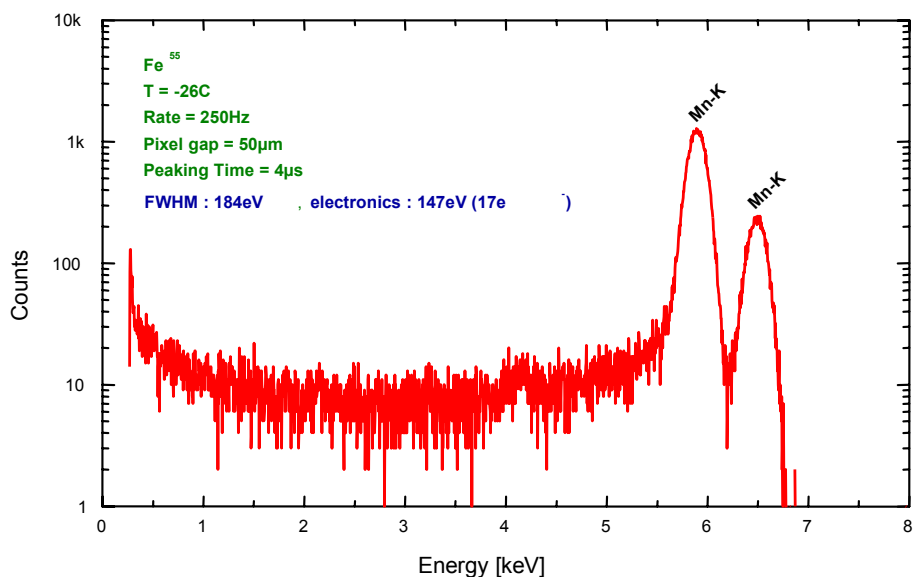

Fig. 3   Energy resolution of 184 eV FWHM (Mn Ka) measured for a single Si pad detector at -26 °C and 250 Hz using a ^{55}Fe source [3].

References

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[6] Research carried out (in whole or in part) at the National Synchrotron Light Source, Brookhaven National Laboratory, which is supported by the U.S. Department of Energy, under Contract No. DE-AC02-98CH10886, and through the CSIRO Synchrotron Business Development Project.