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First Measurement Results of new SDD Detectors with DEPFET Based readout Node and Minimized Input Capacitance

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The combined detector-amplifier structure DEPFET [1] (Depleted P-channel FET) increasingly finds application as basic building blocks for radiation detectors in a large variety of scientific fields, e.g. as focal plane detector for space borne X-ray telescopes [2]. Fig. 1 shows a cutaway of a circularly shaped standard DEPFET cell. It consists of a p-channel FET with a potential minimum for electrons located directly beneath the transistor channel, where bulk-generated charge is collected. The transistor current becomes a function of the charge in the potential minimum (the so-called *internal gate*), This configuration has an equivalent readout capacitance lower than 20 fF.

Reducing the analysis time in EDX applications has always been one of the top priorities for SDD detector developments in the field of microanalysis. As high photon throughput is the key performance parameter, and as the effective input capacitance of the readout node has the biggest impact on the SDD performance, minimizing this parameter is the most efficient way to boost photon throughput while maintaining outstanding spectral performance. Here, SDD Devices with DEPFET based readout nodes, so-called DSDDs, open up new possibilities.

The advent of the Silicon Drift Detector Droplet (SD3) with its modified low capacitance readout node already demonstrated impressively the performance scaling power of the input capacitance. Later, the introduction of a new generation of state-of-the-art SDD devices with unprecedented performance was made possible by topological optimizations of the structure of readout anode and integrated JFET allowed to reduce the input capacitance even further. And this is, where DSDD devices could allow for another leap in performance.

DSDD devices combine the traditional advantages of SDDs, like scalability and optimized QE, with the advantages of the DEPFET cell, e.g. low input capacitance and charge storage capability. Due to their compact design, they have the potential for further miniaturization, which comes along with an additional decrease of capacitance. Current standard prototypes, implementing a conventional DEPFET design, already exhibit with 125 eV FWHM for 5.9 keV at -20°C and 1 μs of shaping time performance values comparable to state-of-the-art SDDs (figure 2). In addition, they show a very good performance at elevated temperatures due to inherent advantages in the production technology and specific design features (figure 3). A spectral resolution of 141 eV FWHM at 5.9 keV and 1 μs of shaping time has been measured at 20°C. Another advantage is the possibility to add functionality to the pixel. One example here is the implementation of a fast electronic shutter, i.e. the possibility to control the sensitivity of the device to X-rays by an electronic contact with a time resolution in the 10 ns scale. Prototyping devices including this and other features have been manufactured [3], proof-of-principle measurements have been made and will be reported.

References:

[1] J. Treis et al., *IEEE TNS,* 52 (Iss 4), (2005) p. 1083.
[2] J. Treis et al., *JINST,* 4 (2009) p. 03012.
[3] A.Bähr et al., *Proc. SPIE* 8453, 84530N (2012).

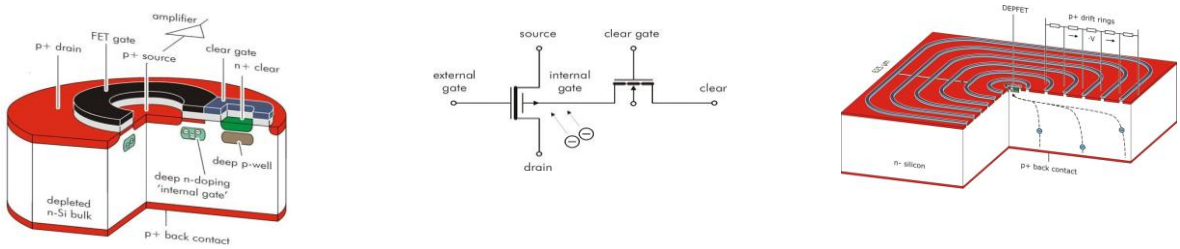

Fig. 1. Cutaway (left) of a standard DEPFET cell. The charge is stored in a dedicated potential minimum for charge directly underneath the external gate. The stored charge can be removed by the additional n-channel ClearFET. The circuit schematic (middle) shows the basic functionality: a P-channel FET with two gates: an external and an internal gate, where the latter one is contacted with an additional N-channel FET. The DEPFET cell can replace the standard readout anode of an SDD.

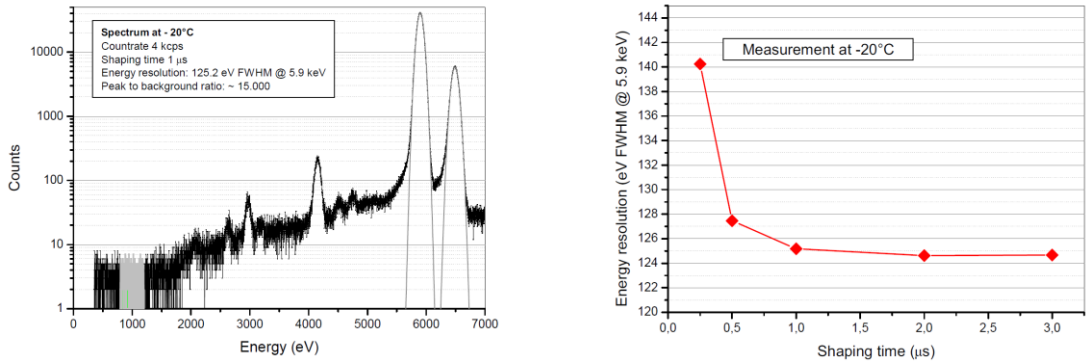

Fig. 2. Performance of an DSDD device at -20 °C. The optimum energy resolution of ~ 125 eV FWHM @ 5.9 keV is achieved at shaping times of between 1 and 2 µs and is compatible to the performance of an SDD^{plus} device.

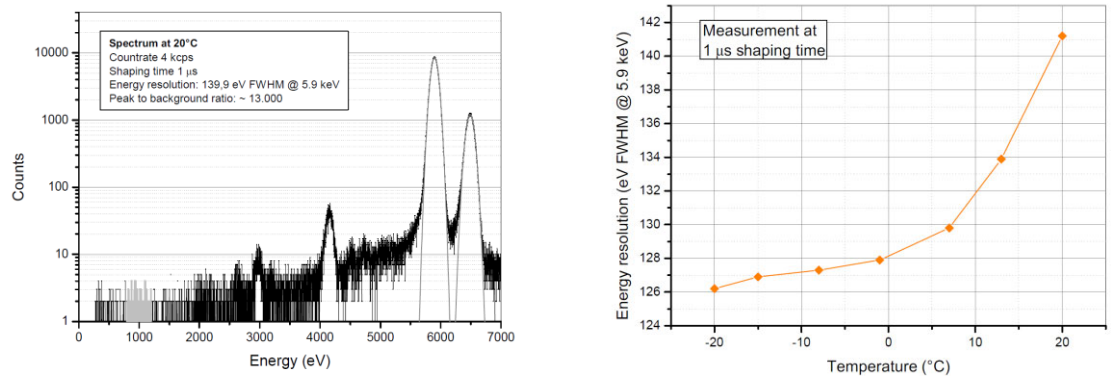

Fig. 3. Performance of the same DSDD device at room temperature. Due to inherent technological advantages in the manufacturing process, leakage current contributions can be efficiently suppressed, resulting in an energy resolution of ~ 141 eV FWHM @ 5.9 keV for1 µs shaping time at 20° C.

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