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2D Junction Profiling on Semiconductor Device Reliability Fail

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Dual lens Electron Holography (DLEH) and scanning capacitance microscopy (SCM) measurement has been shown to be effective methods to measure junction profile in recent years for semiconductor research and manufacturing process. However, due to the sample preparation difficulty and data interpretation, these two methods are not commonly used as a tool for the physical defects analysis. In this presentation, we will demonstrate that by applying these two techniques on the same defects analysis, better understanding of dopant related defects and failure mechanisms can be derived as well as more effective data interpretation from each technique.

In electron holography, electric potential is measured by measuring the phase difference between N-doped and P-doped regions of the semiconductor devices [1-4]. Scanning capacitance measures the slope of CV curve in a MOS capacitor structure formed by a conductive AFM probe and an oxidized semiconductor surface to provide charge carrier type and relative concentration [5,6].

In this report, electron holography is carried out on a dual lens holography system with 200kV (1-4) and sample is prepared by focused ion beam (FIB) method to about 400 nm thick. An NFET SOI device is stressed by applying high voltage (3.1V) from source to drain for approximately 10,000s as shown in fig.1. The drive current of the device changes (reduces) about 7.3% after stress as shown in fig.2.

Figure 3 shows electric potential measured by dual lens electron holography. The colored map in Si shows asymmetry of junction profile from left to right. The left side junction is more abrupt and right side junction is less abrupt. Figure 4 show the electric potential profile in the channel region (top part of Si) from left to right, which indicates the similar asymmetry between left and right. The device without stress has a symmetric junction.

Scanning capacitance measurement on stressed sample is shown in (fig.5). The color contrast shows an asymmetric junction profile between drain side and source side of the channel. A lateral 1D profile taken through the channel (fig.6) clearly shows a large SCM signal at the left junction compared to the right junction. The signal difference indicates a carrier concentration difference between the two ends of the channel after device stress.

In conclusion, both electron holography and scanning capacitance measured on the same defective device shows junction asymmetry, with the junction on drain side to be more abrupt than one on the source side after the 10,000 second device reliability stress.

References:

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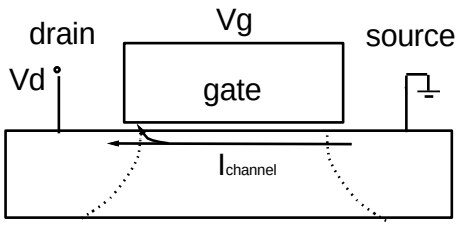
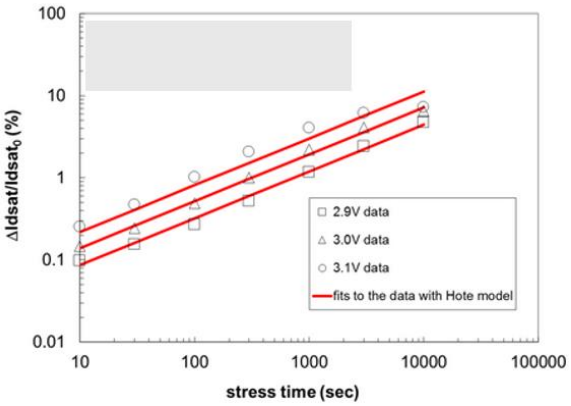
Figure 1.



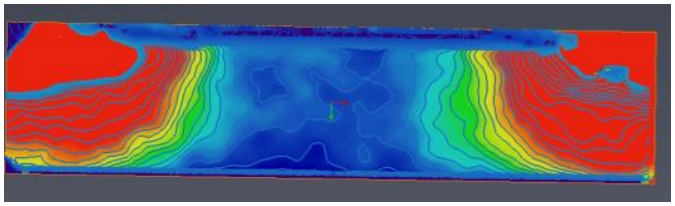
Electric circuit diagram for hot carrier stress

Figure 2.



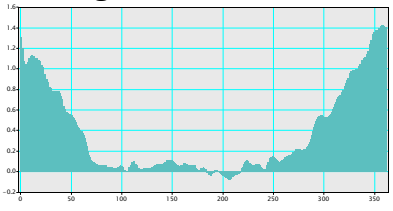
Device drive current change vs stress time with different stress voltage

Figure 3.



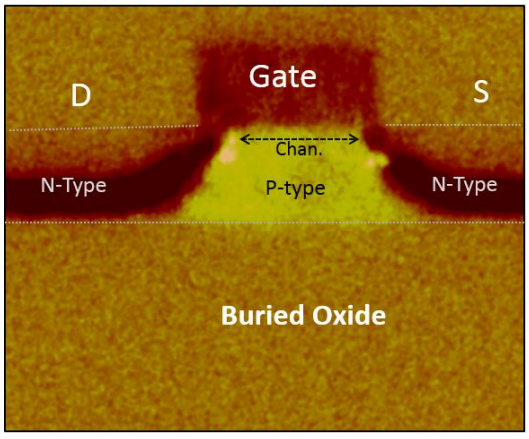
Junction profiling by dual lens electron holography

Figure 4.



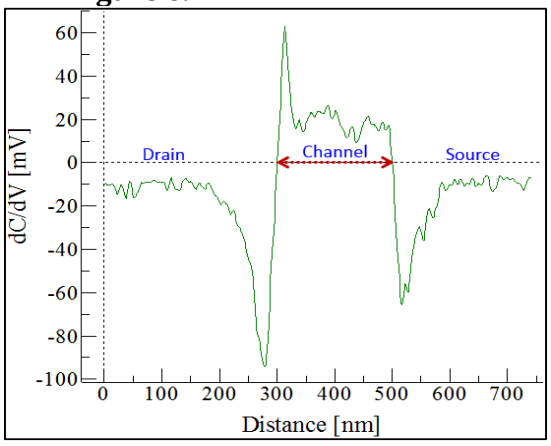
Electric potential profile near the top of channel

Figure 5.



Scanning capacitance map on stressed device

Figure 6.



Profile of SCM near the top of the channel.

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