

## HRTEM Study of Lithographically Defined Silicon Nanowires

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Display technology is heavily used in modern society, from picture frame liquid crystal display (LCD) screens in homes to projectors for presentations in businesses. Researchers are constantly attempting to create more efficient displays out of materials that cost less. It is known that bulk silicon is a minimal cost material but does not emit visible light. Only when its dimensions are scaled down into the quantum regime is it able to efficiently display visible colors [1]. Silicon nanowires exhibit quantum effects with their dimensions reduced from 3-D to 1-D. To obtain such dimensions, researchers have used fabrication methods such as synthesis and lithography [2-3]. In this study, we use electron beam (e-beam) lithography to fabricate silicon nanowires with axial directions along [1-10] or [100] and widths smaller than 10nm, as seen in Figure 1(a).

The silicon nanowires used in this study were fabricated from silicon on insulator (SOI) wafers. These wafers contained a 10nm single crystal Si layer on a 150nm buried oxide (BOX) and Si substrate. E-beam lithography was used to pattern an HSQ resist on the wafer with a 3nC/cm exposure dose. These patterns contained lines that run along the <100> and <1-10> zone axes. It was then developed in a 25% tetramethylammonium hydroxide (TMAH) solution at 45 degrees C for a minute. The Si layer on the BOX was then etched by inductively coupled chlorine plasma, leaving Si nanowires on the BOX surface. One sample wafer went through controlled oxidation to reduce and compare their sizes. The wafers were prepared for transmission electron microscopy (TEM). Using the focused ion beam (FIB) lift-out technique we were able to view the nanowires in cross-section.

As-fabricated nanowires are shown in Figure 2. Figure 2(a) is a nanowire fabricated along the [1-10] crystallographic orientation, where its cross-sectional shape of a well-defined ~10nm by ~10nm square is expected of the plasma etch. Figure 2(b) is a nanowire fabricated along the [100] crystallographic orientation, also as a ~10nm by ~10nm square. Figure 2(a) and (b) are images taken of the [1-10] and [100] oxidized nanowires, respectively. The [1-10] nanowire had its width reduced to ~6nm and the [100] reduced to ~4nm. It is interesting to note that the [1-10] sample had a slower non-uniform oxidation along its plasma etched sidewall, while the [100] sample had a quicker perfectly uniform oxidation, preserving its straight edges.

This lithography approach for nanowire fabrication provides a top-down method that allows us to control their orientation and size. In the same manner, future nanowires can be fabricated using different materials, such as Ge, GaAs and Ge on Si. This will allow for exploration of these materials properties when scaled down to the quantum regime. Scaling can also be done to reduce materials down to zero dimensions, essentially fabricating quantum dots that are single crystal and positioned according to the e-beam lithography pattern, as shown in Fig. 1(b). With this ability, visible light emission from silicon quantum dots will hopefully be observed [4].

[1] A. G. Cullis and L. T. Canham, Nature 353 (1991) 335

[2] H. Suzuki et al., Chem. Phys. Lett. 468 (2009) 211

[3] M. Jeon et al., *Mater. Lett.* 63 (2009) 246

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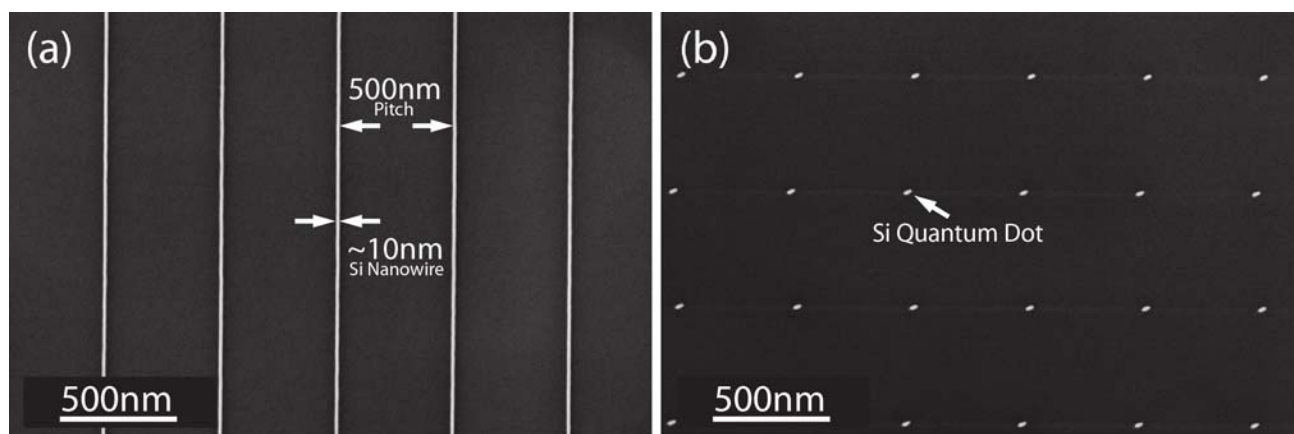


Fig. 1. SEM images of the Si (a) nanowires and the (b) quantum dots.

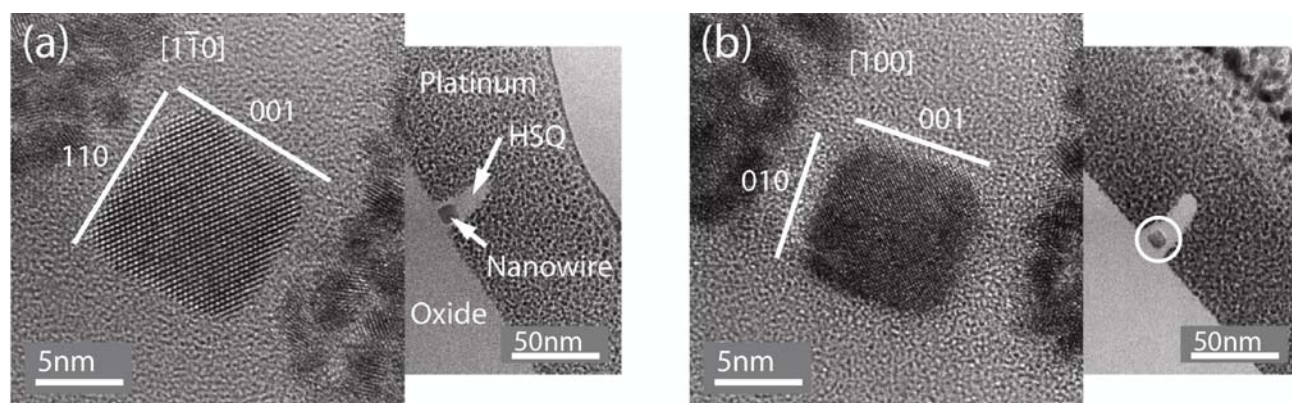


Fig. 2. Cross-sectional HRTEM images of nanowires patterned along the (a) [1-10] and (b) [100] crystallographic directions. Both are ~10 nm in width and height.

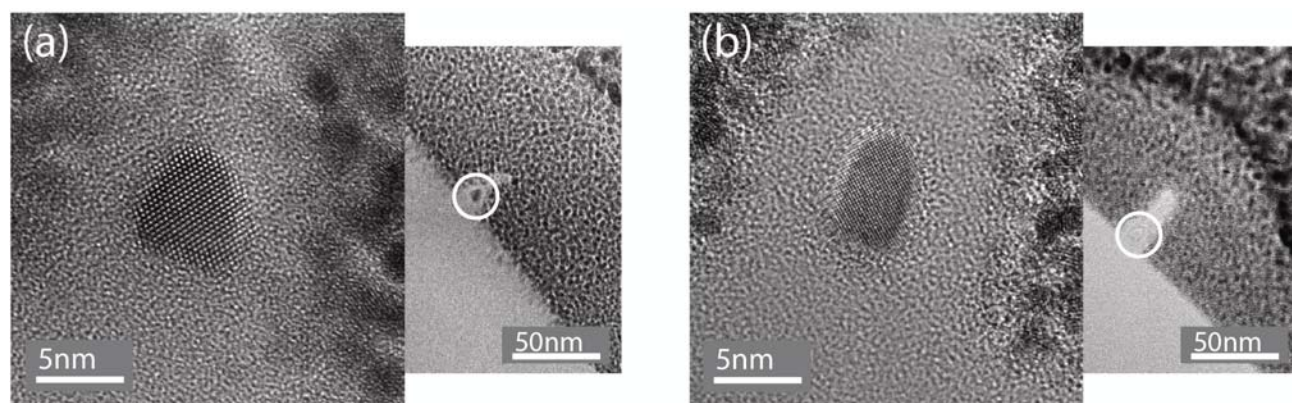


Fig. 3. Cross-sectional HRTEM images of nanowires patterned and then oxidized along (a) [1-10] and (b) [100] orientations. The [1-10] nanowire oxidized at a slower rate than the [100]. The [100] nanowire also oxidized uniformly down its sidewall, keeping its rectangular shape.