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Quantitative Strain Measurement in Semiconductor Devices by Scanning Moiré Fringe Imaging

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Strain engineering is widely used for the enhancement of carrier mobility in electronic devices made up of transistors. To obtain optimized electrical performance, one must measure the strain field that is formed in the channel region of the transistor. As these devices continue to be miniaturized, we need to develop techniques that can measure the strain field at nanometer-scale resolutions.

In the present work, we present the strain measurement of a strained-channel transistor using the scanning Moiré fringe (SMF) technique within high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) [1-4]. Figure 1(a) shows an illustration of the SMF formed by harmonic interference between the scanning grating and the crystal lattice. In a HAADF-STEM image, the SMFs appear when the scanning grating spacing d_s is close to the crystal lattice spacing d_l [1]. The SMF spacing d_{SMF} decreases as the crystal lattice spacing decreases for $d_l < d_s$ [2]. Figure 1(b) shows a variation of the d_{SMF} as a function of the strain field (d_s = 0.1979 nm). Because the d_{SMF} is very sensitive to local changes in the crystal lattice plane, the strain field in the crystal structure can be estimated simply by measuring d_{SMF} for a calibrated value of d_s [2].

Figure 2(a) is a high resolution (HR) STEM image of a p-type channel transistor with SiGe-stressors embedded in source and drain (S/D) regions. It should be noted that the atomic columns were visible in the image, as shown in the inset. The lattice parameter of the SiGe is larger than that of pure Si; this induces compressive strain in the channel region. Figure 2(b) shows an SMF image of the transistor formed by the interference between the scanning grating and the lattice spacing of the (220) planes. The SMF image was recorded at d_s = 0.1979 nm. The d_{SMF} was observed to increase in the S/D regions whereas it contracted in the channel region. Thus, the compressive strain field is clearly formed in the channel region of the transistor. To obtain the quantitative strain field in the transistor, d_{SMF} was measured along the [001] direction. Based on the calculation of Fig. 1(a), the measured d_{SMF} values were converted into strain values. The strain values are indicated by the solid line in Fig. 2(d). The strain field in the channel region was estimated to be 1.0%, which decreased toward the Si substrate.

To verify the strain values measured by SMF imaging, we independently performed strain measurement using geometrical phase analysis (GPA) [5] of the high-resolution STEM image; the results are shown in Fig. 2(c) [3]. The strain profile extracted from the strain map using the STEM-GPA method was indicated by the dashed line in Fig. 2(d). As a result, the strain values measured by the SMF image match the result obtained using the STEM-GPA method.

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Our work presents a quantification method for strain measurement using SMF imaging and its application to strained-channel transistors. We suggest that SMF imaging is a useful method that can optimize layout design for strain engineering in nanometer-sized semiconductor devices.

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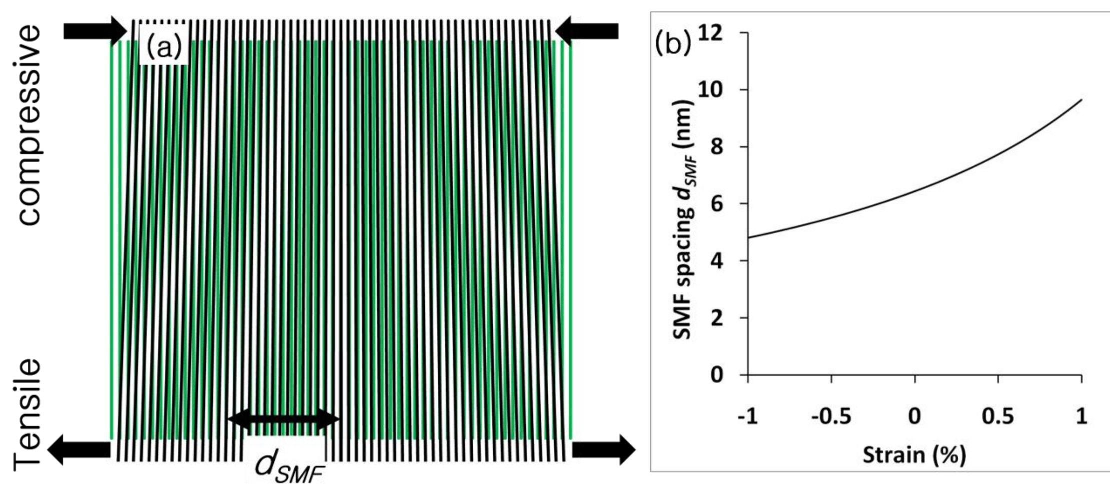

Figure 1. (a) An illustration of SMF by superposition of the strained crystal lattice and scanning grating. (b) The SMF spacing *(d_{SMF})* as a function of strain field calculated at d_s = 0.1979 nm.

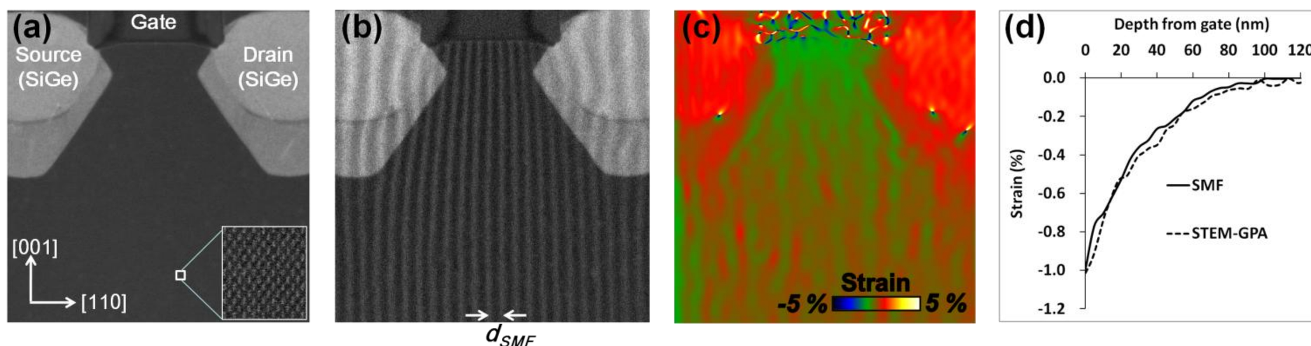

Figure 2. (a) STEM image of a strained-channel transistor. (b) SMF image of the transistor. (c) Strain map obtained using STEM-GPA method. (d) Strain profiles extracted from SMF and STEM-GPA images.

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