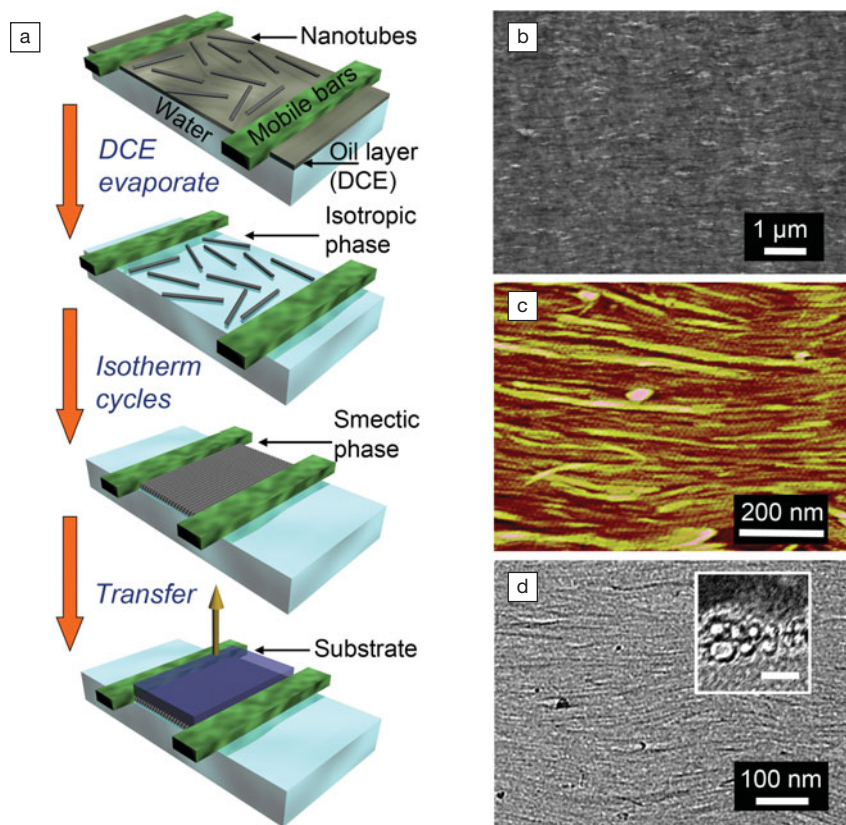


**Nano Focus**
**Langmuir–Schaefer assembled carbon nanotube arrays show superior electronic properties**

With their exceptional electronic properties, single-walled carbon nanotubes (SWCNTs) have the potential to replace silicon in thin-film transistors and high-performance logic devices. However, such applications require densely packed arrays of aligned SWCNTs for sufficient current and/or power output. Although dense, aligned SWCNT arrays have been grown on crystalline substrates using chemical vapor deposition, obtaining pure semiconducting nanotubes from the resulting mixture of metallic and semiconducting SWCNTs is problematic. An alternative approach is to separate the metallic and semiconducting SWCNTs in solution, and then assemble the semiconducting nanotubes into arrays. Assembly using shear force or electric fields, however, results in low nanotube density ( $<50$  nanotubes/ $\mu\text{m}$  or about 10% surface coverage), which provides insufficient current density. Q. Cao and a team of researchers at the IBM T. J. Watson Research Center have now used a Langmuir–Schaefer method to create densely packed, aligned arrays of 99% pure semiconducting SWCNTs with nearly full surface coverage. Transistors fabricated with these SWCNT arrays displayed current densities  $>120 \mu\text{A}/\mu\text{m}$ , transconductances  $>40 \mu\text{S}/\mu\text{m}$ , and on/off ratios  $>1000$ —all of which offer substantial improvements over previously reported devices comprising integrated carbon nanotube channels.

As reported in the January 27 online issue of *Nature Nanotechnology* (DOI: 10.1038/NNANO.2012.257), an isotropic two-dimensional nanotube film was formed at the air–water interface by dispersing a concentrated 99% pure semiconducting SWCNT solution on a water subphase (see Figure a). The nanotubes were then compressed into well-ordered, two-dimensional arrays using mobile barriers (see figure). Horizontal transfer of the nanotube arrays onto the target substrate for device fabrication produc-



(a) Schematic of the Langmuir–Schaefer assembly process is shown. Images of aligned nanotube arrays transferred onto solid substrates obtained with (b) scanning electron microscopy, (c) atomic force microscopy, and (d) top-view transmission electron microscopy (TEM). The inset of (d) is a high-resolution cross-sectional TEM image, with a scale bar representing 5 nm. DCE is 1,2-dichloroethane. Reproduced with permission from *Nature Nanotech.* (DOI: 10.1038/NNANO.2012.257). © 2013 Macmillan Publishers Ltd.

es better alignment and higher yields than the vertical transfer in the Langmuir–Blodgett method because of the reduced disturbance of the film on water.

Characterization of the SWCNT films showed that the nanotubes fully covered the substrates as a uniform double layer. The nanotube pitch is self-limited by the nanotube diameter plus the van der Waals separation, leading to a tube density as high as 1100 tubes/ $\mu\text{m}$  in this work. By fabricating a device on a 10 nm  $\text{HfO}_2$  gate dielectric with channel dimensions of 120 nm length and 100 nm width (with current traveling along the length) so that only about 110 nanotubes are present, the researchers were able to fabricate transistors containing only semiconducting SWCNTs. These devices exhibited the highest transconductance and current density reported to date for SWCNT arrays—a threefold

increase over devices with the same geometry but with nanotube arrays with moderate tube density, together with high on/off ratio. The greatly decreased nanotube separation does not affect the SWCNTs' intrinsic properties, but makes it more challenging to form high-quality electrical contacts between each SWCNT inside the array with metal source/drain electrodes.

The researchers said, “Improvement in the electrical contact between the nanotube arrays and metal electrodes, further optimization of the nanotube electronic type and diameter separation techniques, reduction of interface traps for better device consistency, together with complementary metal–oxide–semiconductor-compatible circuit- and system-level implementation, represent important subjects for future work.”

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