

Electrostatic gating of hybrid halide perovskite field-effect transistors: balanced ambipolar transport at room-temperature

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(Received 29 March 2015; accepted 16 April 2015)

Abstract

The hybrid halide perovskites combine the low-cost processing characteristics of organic materials with the performance factors of inorganic compounds. Recently the power conversion efficiencies of perovskite photovoltaic solar cells have reached a respective value of ~20%. The charge transport properties were indirectly approximated in these compounds because of lack of available field-effect transistors (FETs). Here we report the fabrication and room-temperature operation of FETs based on the hybrid perovskites. We obtained balanced electron and hole transport with mobilities of ~1 cm²/Vs. We also found that the yield, as well as the operational and environmental stability of the fabricated transistors is limited.

Inorganic perovskite materials have attracted significant research effort given their rich physical properties that includes high-temperature superconductivity, colossal magnetoresistance, ferroelectricity, diverse magnetic properties, etc.^[1,2] Their structure has the general formula ABX₃, where the cation B resides in the center of the corner sharing BX₆ octahedra, the X anions occupy the corners; whereas cation A is surrounded by eight such octahedra (see, for example, SrTiO₃, YMnO₃, YVO₃, and LaMnO₃). The newest member of the perovskite family, namely the organic–inorganic perovskites, have recently emerged as an intriguing class of materials, which combine the low-cost processing and versatility characteristics to organic materials with the performance factors of inorganic compounds.^[3,4] In particular, organo-lead halide perovskites (A⁺PbX₃), where A⁺ is the organic cation and X denotes the halogen atom, have quickly become one of the hottest topics of research these days, in spite of the concerns related to the environmental hazard posed by the lead component. For example, the power conversion efficiency of hybrid perovskite photovoltaic (PV) solar cells has exceeded 19%,^[5] and the light-emitting diodes (LEDs) based on these compounds rival the best on the market.^[6] In addition, hybrid perovskite semiconductors exhibit wavelength-tunable photoluminescence (PL) emission,^[7]

laser action,^[8] and charge carrier diffusion lengths of the order of hundreds of micrometers.^[9] Surprisingly, these compounds also show interesting spin-related properties, including magneto-photocurrent, magneto-electroluminescence, and magneto-PL, in spite of their fast spin relaxation that is due to the strong spin–orbit coupling.^[10,11] The hybrid perovskites based on methylammonium (where A⁺ = CH₃NH₃⁺) are most common, but other organic cations, such as ethylammonium CH₃CH₂NH₃⁺ or formamidinium NH₂CH = NH₂⁺ have also been explored.^[12,13] It has been found that the anion (X = I, Br, Cl) impacts a variety of physical properties such as the crystal quality,^[14] band-gap,^[15] PV solar cell efficiency,^[16] exciton-binding energy^[17] and the amplified spontaneous emission wavelength.^[8] Mixed halide perovskites such as CH₃NH₃PbI_{3-x}Cl_x, offer the possibility of fine tuning the physical properties that result from optimized film morphology,^[18] and, in general exhibit higher conductivities and longer carrier diffusion lengths.^[4]

The most exciting breakthroughs of hybrid halide perovskites are without a doubt in the area of PV technologies, where the new records in power conversion efficiencies have been reported at an unprecedented pace; in few years from the first report, the efficiency has improved by more than five times.^[5,19–21] Necessary prerequisites for a material that forms an efficient solar cell are strong optical absorption and efficient charge carrier transport. Whereas the absorption spectrum has been routinely measured directly by the standard optical spectroscopy,^[3,9,22] the charge transport properties

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An earlier version of this article published with authors listed in the incorrect order.
For more information see doi: 10.1557/mrc.2015.33.

were indirectly approximated from space charge-limited current,^[9] Hall effect^[7] and transient THz spectroscopy measurements.^[23] These measurements have indicated the existence of an ambipolar, relatively high-mobility charge transport in the halide perovskites. This observation was further supported by the high-power conversion efficiencies measured in solar cell configurations where the hole-transporting layer is absent,^[24] as well as by theoretical predictions.^[7] Success in the fabrication of hybrid halide perovskite field-effect transistors (HHP-FETs) would unambiguously clarify the nature of charge transport in this class of materials, and promote the development of complementary optoelectronic applications, provided that the device performance is sufficiently high. In spite of several attempts on electrostatic gating of hybrid perovskite FETs, success has been rather limited.^[25–27] In this paper, we report on the fabrication and room-temperature operation of FETs based on the halide hybrid perovskites. We obtained balanced electron and hole transport, in agreement with the high efficiency of PV cells based on these compounds, having mobilities of $\sim 1 \text{ cm}^2/\text{Vs}$. We also found that the device fabrication yield, as well as the operational and environmental stability of the fabricated transistors is limited at the present time.

The crystal structure of the hybrid lead halide perovskites is shown in Fig. 1(a). The lead (yellow spheres) and halide (I/Cl, magenta spheres) occupy the sites at the centers and corners of the octahedron, respectively, whereas the organic cation sits in the interstices. Bottom-contact, top-gated FETs were fabricated on Au-patterned source and drain electrodes that were placed on an insulating substrate [see Fig. 1(b)]. The contacts were defined by photolithography and deposited using e-beam evaporation and lift-off. The substrates were cleaned in hot acetone and hot isopropyl alcohol, followed by UV-ozone and deionized water rinse. Prior to the deposition of the hybrid perovskite semiconductor layer, the electrodes were treated with 2,3,5,6-tetrafluoro-4-(trifluoromethyl)benzenethiol (TTFB, Sigma Aldrich) self-assembled monolayer (SAM) by immersing the substrate in a 50 mM solution in Ethanol (Sigma Aldrich)

for 30 min, followed by ultrasonication in ethanol for 2 min. Subsequently, the perovskite layer was deposited from a precursor solution obtained by mixing of 0.8 g of $\text{CH}_3\text{NH}_3\text{I}$ (Dyename) with 0.23 g of PbI_2 and 0.42 g of PbCl_2 (Sigma Aldrich) in 2.5 mL *N,N*-dimethylformamide solvent. The obtained solution was allowed to stir overnight on the hotplate at 70°C in a nitrogen-filled glovebox (H_2O , $\text{O}_2 < 1 \text{ ppm}$). Once cooled to room temperature, the bright yellow solution was spun coated on the pre-fabricated transistor substrates at 2000 RPM, a process that took place in the same glove-box. Subsequently, the films were annealed at 90°C for 15 min, followed by a second annealing step at 105°C for 120 min; this resulted in a change in color to a dark brown, indicating the formation of the $\text{CH}_3\text{NH}_3\text{PbI}_{3-x}\text{Cl}_x$ perovskite layer. This was also confirmed by the UV-vis absorption and PL emission spectrum from the films [see Fig. 2(a)], which are in agreement with those previously measured on such films.^[20,22] The perovskite film shows a broad absorption spectrum down to the near-infrared range, whereas its PL band that peaks at $\sim 770 \text{ nm}$ reveals an optical gap of $\sim 1.6 \text{ eV}$. The absorption tail at energy below the optical gap is probably due to optical transitions into band tail states (i.e., Urbach edge) caused by traps and defects in the film, of which densities increase in thin perovskite films due to excess grain boundaries.^[28] The x-ray diffraction (XRD) pattern [Fig. 2(b)] shows mainly the [110] and [220] diffraction lines, which originate from the preferential orientation of perovskite crystal domains, in agreement with high-quality solution-processed or co-evaporated films described in the literature.^[29]

For the gate dielectric, a fluoropolymer—Cytop (Asahi Glass) layer was deposited from an un-diluted solution by spin coating in a nitrogen glove-box. The samples were subsequently annealed at 50°C overnight in a vacuum oven to ensure crosslinking of the dielectric layer. Finally, Al top-gate electrode was deposited by thermal evaporation through a shadow mask [see Fig. 1(b) for the final device structure]. The samples were exposed to air between the different steps of the device processing.

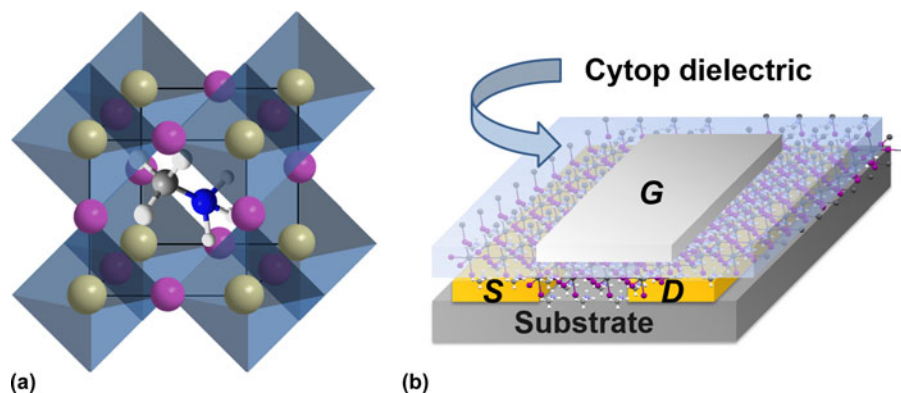


Figure 1. (a) The crystal structure of $\text{CH}_3\text{NH}_3\text{PbI}_{3-x}\text{Cl}_x$ hybrid halide perovskite. The lead (yellow spheres) and halide (I/Cl, magenta spheres) sit at the centers and corners of the octahedron, respectively, and the organic cation sits in the interstices. (b) Schematic structure of the FETs based on hybrid halide semiconductor layer, having Au source and drain contacts, Cytop dielectric and Al gate electrode.

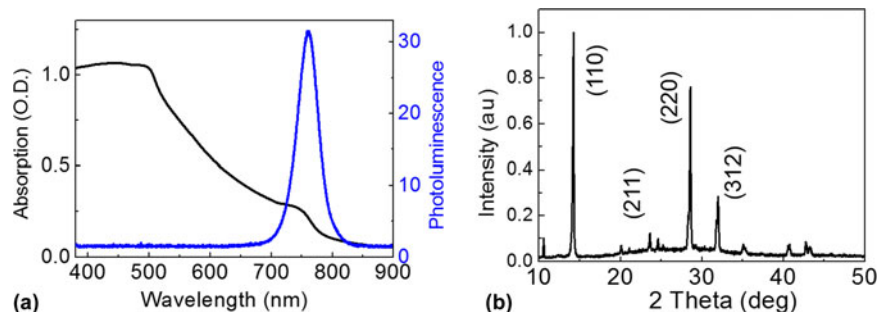


Figure 2. (a) Absorption (black) and PL (blue) spectra of a $\text{CH}_3\text{NH}_3\text{PbI}_{3-x}\text{Cl}_x$ film used in the FET studies. (b) The XRD pattern on a similar film.

Figure 3 shows current–voltage (I – V) characteristics for a FET device having channel length, $L = 30 \mu\text{m}$ and channel width, $W = 1000 \mu\text{m}$. All measurements were performed in air, using an Agilent 4155C semiconductor parameter analyzer (with a voltage step of 0.2 V and using short integration time to minimize the bias stress effects). In Fig. 3(a), we plot the I – V characteristics measured at source–drain voltage, $V_{\text{DS}} = -30 \text{ V}$, where p-type transport is detected. The relatively noisy nature of the curves most probably originates from the fact that the measurement was fast, to prevent device degradation because of bias stress. A hole mobility, $\mu_{\text{h}} = 1.3 \text{ cm}^2/\text{Vs}$ was calculated from the square-root dependence of the drain current I_{D} versus the applied source–gate voltage, V_{GS} (blue curve) using Eq. (1) below, where C_i is the dielectric capacitance per unit area ($C_i = 1.3 \text{ nF}/\text{cm}^2$, estimated based on the $1.4 \mu\text{m}$ dielectric thickness, and using a dielectric constant value of $\epsilon_r = 2.05$, as quoted by Asahi Glass Co.):

$$\mu_{\text{h}} = \frac{2L}{WC_i} \left(\frac{\partial \sqrt{I_{\text{D}}}}{\partial V_{\text{GS}}} \right)^2. \quad (1)$$

As this curve shows deviations from a straight line, in Figs. 3(a) and 3(b) we marked in red the voltage range used in mobility estimation. The on/off ratio and the subthreshold slope, S , extracted from this I – V dependence were measured to be:

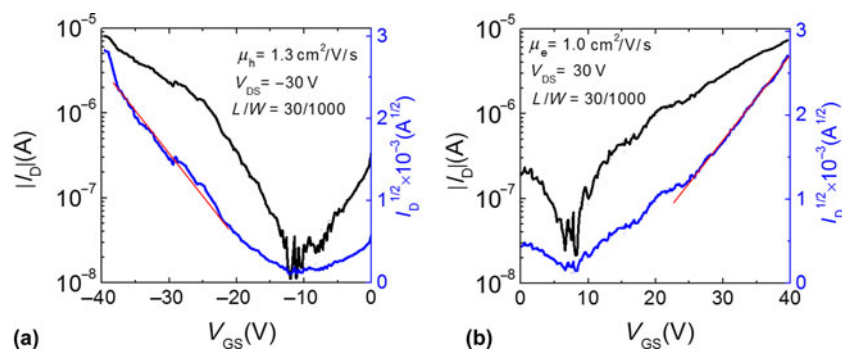


Figure 3. Transfer I – V characteristics for the p-type transport (a) and n-type transport (b) in HHP-FETs. The drain current is plotted versus the gate voltage in black, and the square root of the drain current value is plotted in blue. The slope used in mobility estimation is shown in red.

on/off = 10^2 and $S = 2.1 \text{ V}/\text{dec}$, respectively. The same device also showed electron transport [Fig. 3(b)] with an extracted mobility $\mu_{\text{e}} = 1.0 \text{ cm}^2/\text{Vs}$, on/off ratio of 10^2 and $S = 1.5 \text{ V}/\text{dec}$. While the mobility and subthreshold slopes of our HHP-FET devices are on par with those of the best-reported organic FETs, the on/off ratio is significantly lower, most probably because of the relatively large off-current in the device due to the fact that the perovskite layer was not patterned.

FET devices with higher mobilities were also obtained; however, these values resulted from non-ideal transfer characteristics. For this reason we limit our discussion to a conservative estimation of the charge carrier mobility. We also notice that the FET device yield is low so far, mostly because of the challenges in controlling the film wetting on the very hydrophobic surface created by the TTFB treatment (with water contact angle of 107°). Work is in progress to understand this phenomenon, and improve the FET yield. Another possible reason for the low device yield is the partial degradation of the hybrid perovskite films prior to Cytop deposition. The modest robustness of the hybrid perovskite layer to environmental exposure is a well-known issue.^[5] Cytop dielectric should also serve as an encapsulation layer; however, we noted that the devices degrade during several hours regardless of the storing conditions (vacuum, glove-box, and ambient air were tested). On the bright side, we found that some FET devices maintained good performance for several days; we are currently

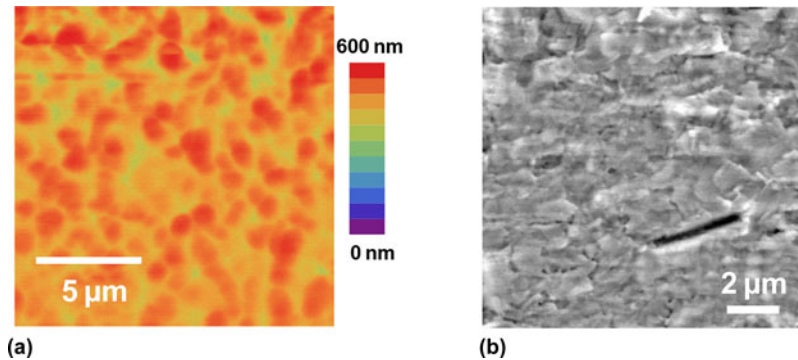


Figure 4. (a) AFM measurements of a $\text{CH}_3\text{NH}_3\text{PbI}_{3-x}\text{Cl}_x$ film used in this study. (b) SEM measurements of a similar film.

designing systematic experiments to understand this behavior. FETs on bottom SiO_2 gate dielectric were also fabricated, but unfortunately no transistor behavior has been observed from such devices. For comparison, we also fabricated devices with Cytop dielectric, but without the TTFB contact treatment. We found that the yield in these devices is even lower, and the obtained transistor characteristics are not ideal, showing a sharp turn-on, followed by a lower slope, which is typically attributed to contact resistance. The maximum charge carrier mobility extracted from such devices was of the order of $0.1 \text{ cm}^2/\text{Vs}$; however, because of the nature of the non-ideal I - V curves, we believe that this is an overestimation.

To understand the impact of the electrode surface chemical modification on the charge injection and transport, we estimated the shift in the work-function using Kelvin probe technique. A detailed description of this technique can be found in Ref. 30. We found that an increase of $0.41 \pm 0.02 \text{ eV}$ was introduced upon SAM treatment, establishing an electrode work-function of $5.32 \pm 0.02 \text{ eV}$. This value explains the successful hole-transport in the transistor channels; however, it cannot explain the electron injection due to the large Schottky barrier that forms here. We note that the conduction band minimum in the hybrid perovskites lies at -3.75 eV , and the valence band maximum is at -5.3 eV .^[31] This observation demonstrates that when dealing with charge transport in HHP-FETs the energy band diagram picture does not always guarantee controlled charge injection. Here, charge injection and collection are probably dominated by the hybrid perovskite film morphology at the interface with the electrodes, and the resulting contact resistance.

The FET mobility values extracted from the obtained I - V measurements are lower than those measured using other electrical methods. The reason for that is that the charge carrier transport in FET devices is not only related to the quality of the perovskite layer, but also to the processes that occur at the semiconductor/dielectric interface, where interface states and low coordination bonds or dangling bonds may also impact conductivity. Excess roughness at this interface can also increase charge carrier scattering, which results in lower mobility. In addition, charge trapping at the grain-boundaries is known to

inhibit charge transport. The perovskite films in our studies show typical roughness of $70 \pm 10 \text{ nm}$, determined from atomic force microscopy (AFM) measurements [see Fig. 4(a)]; and grain sizes of the order of hundreds nm [see the scanning electron microscopy (SEM) image shown in Fig. 4(b)]. We therefore anticipate a substantial increase in mobility when increasing the grain size or working with perovskite single crystals, which may provide with the ultimate degree of order in these systems. We note that post-fabrication treatment using solvent annealing was already shown to increase grain size and enhance carrier diffusion lengths in the hybrid halide perovskites.^[32]

In summary, we fabricated the first successful halide organic-inorganic hybrid perovskite FETs and measured their electrical characteristics at room temperature. We obtained balanced electron and hole-transport with mobilities of $\sim 1 \text{ cm}^2/\text{Vs}$. The processing temperature has not exceeded $105 \text{ }^\circ\text{C}$, which ensures the compatibility with flexible plastic substrates where these devices can be manufactured using fast, large-area deposition methods such as inkjet printing, spray deposition, etc. This first generation devices, however suffer from short lifetimes and performance degradation during operation and/or storage, which may be improved at later time.

Acknowledgments

We acknowledge the Office of Naval research for support. We also acknowledge the Utah NSF-MRSEC for supporting the acquisition and development of the glove-box/metal evaporation facility in the department of P&A at the University of Utah.

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