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TEM Specimen Preparation for Integrated Circuits - Challenges and Solutions

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Transmission electron microscopy (TEM) has become an increasingly powerful technique supporting the development and manufacturing of deep sub-micron integrated circuits (ICs) due to its high resolution and nano-spot analysis capabilities [1]. High precision and fast through-put time (TPT) are the two key factors that will determine if TEM can meet the growing demand from new process development as well as from high volume manufacturing environments where a quick response to process excursion/line down situations is required. A variety of new specimen preparation techniques have emerged to meet these challenges since Marcus and Cheng first demonstrated the feasibility and utility of applying TEM to semiconductors [2]. These techniques can be basically categorized as focused ion beam (FIB) cross-section, wedge (tripod polisher), planar and FIB lift-out methods [3]. Today, a precision cross section TEM specimen can be completed between 2 – 5 hours depending on the complexity of the device feature.

FIB cross-section method: The advent of the FIB technique has brought TEM specimen preparation to a high precision era. From a practical standpoint, overall specimen quality and higher preparation TPT are two major issues associated with the conventional single beam FIB technique. The dual beam-focused ion beam (DB-FIB) system demonstrates superior performance over the single beam system including reduced TPT, ability to precisely section features in the sub micron range, high accuracy for endpoint control, and higher success rates. The newly emerged automatic TEM specimen prep system, Sela's "TEMpro", eliminates manual grinding/polishing for the entire FIB sliver preparation, which is normally performed by a highly skilled expert technician. Our evaluation data showed that the average TPT for sliver preparation is 18 minutes per specimen and the success rate is ~90%. The "TEMpro" can produce standard slivers (~30 μm thickness) from both inline and end of line wafers (0.4 mm and 0.7 mm thickness). Combining with Sela cleave instrument (MC200), the "TEMpro" was able to prepare a site specific FIB sliver (Fig. 1)

Wedge method: Wedge is the most inexpensive technique from the capital investment standpoint. It has replaced the conventional dimple/ion mill method in almost every application area except plan view specimen preparation due to numerous advantages introduced by the wedge method including large transparent area, little or no ion milling damage, and precision [4]. It is also a fast technique suitable for preparing specimens with repeatable structures. Currently, 30% of specimens in our lab are prepared using this method. However, extensive training and exercise is needed to become proficient with this technique. The nearly 100% manual preparation and personnel-dependent operation procedure seems to prevent the adoption of wedge as the primary technique by TEM labs as compared with the DB-FIB cross-section method which offers standard and easy procedures and the added benefit of SEM for monitoring the thinning process.

Planar method: Historically, TEM plan view specimens were made by dimple and ion mill techniques, where a dimple is ground in the back of the specimen behind the region of interest and the balance of the Si is ion milled away. This conventional technique has become increasingly difficult to use to prepare high-precision planar TEM specimens from deep sub-micron devices due to poor optical imaging resolution, non-planar polishing, lack of flexible ion beam control and lack of *in situ* process monitoring for endpoint. Recently, several novel methods employing FIB technology have been developed to prepare high precision planar TEM specimens [5-6]. These methods have been successfully applied to isolate various horizontal sections in MOS (metal-oxide semiconductor) devices such as device channel, gate oxide, spacer/polycrystalline Si sidewall and other transistor features with uniformly thin areas ranging from the single-bit device level to >10 μm long devices. Fig. 2 shows a case where we used this method to identify the root cause for a failed transistor due to high leakage current caused by a Fe particle between poly and spacer.

FIB "lift-out" method: This technique has become increasingly attractive to the TEM community due to the advantage of no mechanical grinding/polishing [7]. The FIB "lift-out" essentially consists of two parts: preparation of a membrane and transfer of the membrane (lift-out) to a grid. A variety of specimens including semiconductor, metal and ceramics have been successfully prepared using this technique. The FIB lift-out method has also been used for plan-view semiconductor specimen preparation. One of the unique applications of this technique is to prepare multiple specimens from within a very small area. This is especially significant during failure analysis (FA) where multi-site sampling is required due to imprecise fault isolation. We have successfully prepared two samples that were 5.5 μm apart from an FA unit using this technique.

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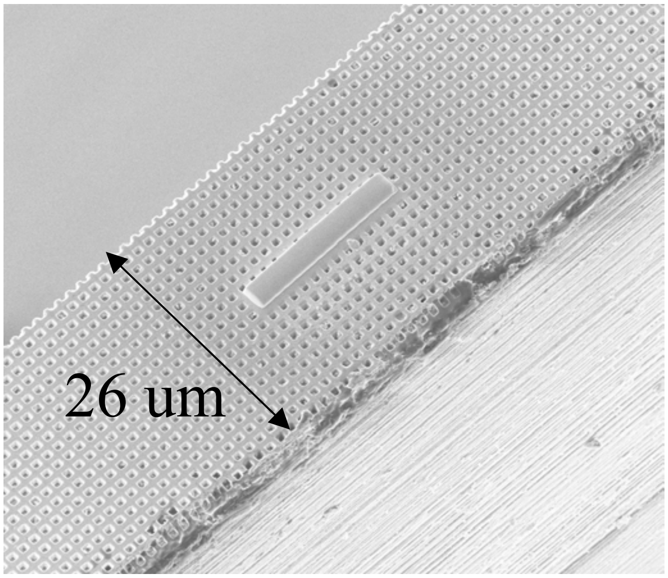

Figure 1. A site-specific FIB sliver prepared by Sela's TEMpro.

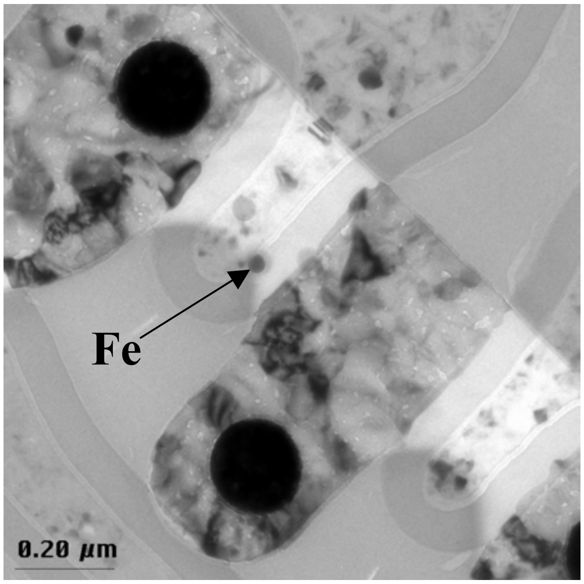

Figure 2. A Fe particle was captured in a high precision planar specimen using the DB-FIB method.