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Reliability analysis of BiCMOS SiGe:C technology under aggressive conditions for emerging RF and mm-wave applications: proposal of reliability-aware circuit design methodology

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Abstract

In this contribution, the impact of extreme environmental conditions in terms of energy-level radiation of protons on silicon–germanium (SiGe)-integrated circuits is experimentally studied. Canonical representative structures including linear (passive interconnects/antennas) and non-linear (low-noise amplifiers) are used as carriers for assessing the impact of aggressive stress conditions on their performances. Perspectives for holistic modeling and characterization approaches accounting for various interaction mechanisms (substrate resistivity variations, couplings/interferences, drift in DC and radio frequency (RF) characteristics) for active samples are down to allow for optimal solutions in pushing SiGe technologies toward applications with harsh and radiation-intense environments (e.g. space, nuclear, military). Specific design prototypes are built for assessing mission-critical profiles for emerging RF and mm-wave applications.

Introduction

In recent years, silicon–germanium (SiGe) technology proved high performances for components with high monolithic integration [1,2], increased speed with low-power consumption. Continuous progress in this technology renders possible large spectrum of applications from radio frequency (RF), microwave to THz [3], which used to be implemented using III–V compound semiconductors (e.g. GaAs-based technologies) (Fig. 1).

In space and defense applications, in addition to standard trade-offs between application driving parameters such as noise, power, linearity, thermal dissipation, environment conditions (e.g. irradiation, harsh thermal variations) put strong constraints on system-level performances in terms of robustness and variability. Thus, analysis, characterization, and predictive [4] modeling of environmental effects on constitutive system-level components/function blocks is of paramount importance.

In the prior art, investigated typical devices encompass both active (MOS and heterojunction bipolar transistors, diodes) and passive samples (transmission lines, interconnects) [5, 6]. When heavy charged particles such as protons traverse a structure with medium energy (from 20 MeV to several hundreds of MeV), particles induce both ionization and atomic displacement (non-ionizing) effects. Then along the path of the incident proton in the material, both ionizing and non-ionizing energy loss modify the oxide/silicon interface (total ionizing dose, TID effect), the junctions, and the silicon bulk properties as displacement damage dose (DDD) effects. Experimental results and simulations reported in the literature have demonstrated that SiGe devices are tolerant to permanent degradation induced by radiation for both TID for several MRad and DDD effects [7–10]. Nevertheless, most of previously published research studies focused on specific device-oriented modeling and characterization, where interactions and couplings between neighboring elements (components, function blocks, subsystems) are generally not addressed. Furthermore, very limited attention is devoted to the effects of extreme environmental conditions on electromagnetically radiating structures such as antennas, which will enable important functionalities such as MIMO, beamforming, and beamsteering [7]. In this contribution, based on representative structures for linear (passive interconnects), non-linear (low-noise amplifier (LNA)), and electromagnetically radiating

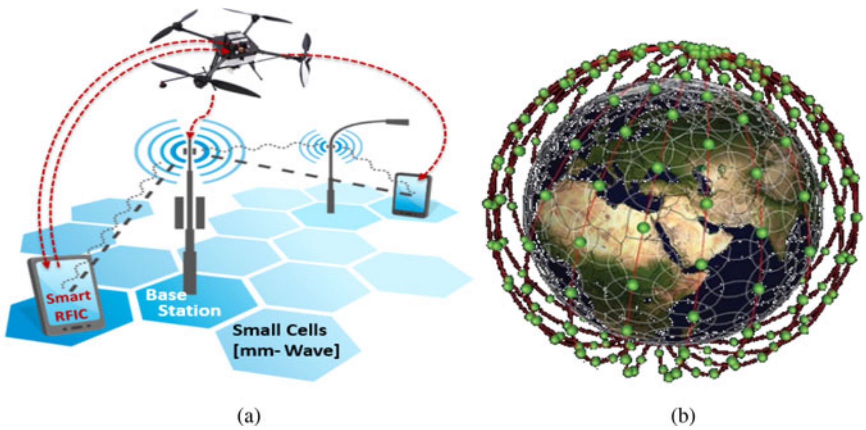

Fig. 1. Use of UAV systems in 5 G as a relay between macro-cell base station and user equipment (a). Low earth orbit (LEO) in the perspectives of Internet Everywhere (b).

elements (antennas), experimental analysis assessing the impact of extreme environmental conditions on the performances of SiGe:C-integrated circuits and systems is proposed in the perspectives of space–defense and emerging 5G mission-critical applications. The contribution is built around two main sections. Section "Experiments in aggressive proton-radiation environmental conditions" describes experiments on passive and active samples in aggressive proton-radiation environments. The third section reports reliability modeling analysis of non-linear components (LNAs). Predictive modeling of degradation effects using in-house tooling solution is compared with the experiments demonstrating satisfactory agreement.

Experiments in aggressive proton-radiation environmental conditions

Designed SiGe BiCMOS passive and active samples were irradiated with monoenergetic (50 and 80 MeV) proton facilities at Kernfysisch Versneller Instituut (KVI). A master sample is used as a reference. Fluencies range from 5×10^{11} to 10^{13} p/cm^2 with a proton flux of 3×10^8 p/cm^2 for lower fluencies and 3×10^9 p/cm^2 for the higher one. Dosimetry of irradiations indicated an accuracy of ±10% for the fluency and ±5% for the proton energy. Two samples were exposed to 53 krad from a Cobalt-60 source at 650 rad/h. Figure 2 gives the equivalent fluencies of 80 MeV protons versus aluminum-shield thickness. These curves are calculated for eight typical space missions ranging from low earth orbits to the GEO orbit.

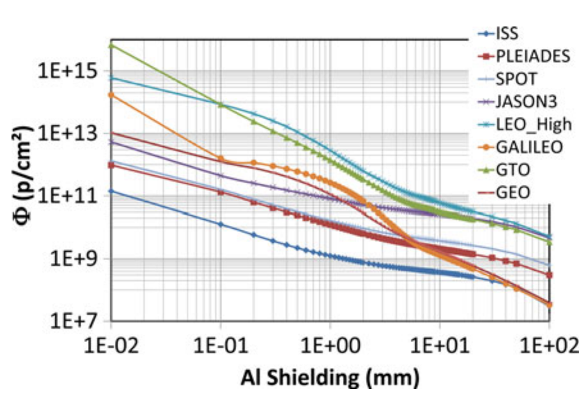

Fig. 2. Equivalent 80 MeV monoenergetic protons fluencies versus aluminum shield thickness for eight typical spatial missions. These fluencies are given for 1-year mission's durations.

The effect of the galactic cosmic rays is neglected because their flux is too weak to induce a significant effect compared with the protons contribution. For the radiation belts models, we use the NASA-Aerospace AE8 and AP8 models in worst-case conditions (i.e. the AE8Max and AP8Min ones). For the mean solar protons model, we use the NASA ESP model with the confidence level set to 85% and we consider that all the missions are done in active period. The mission duration is 1 year for all curves. Figure 4 shows the loss factor of two mm-wave transmission lines (150 and 500 µm long, respectively) and return loss bowtie of coupled antennas (Fig. 3) that were irradiated with protons. The loss factor illustrates the various loss sources (conductive, dielectric, and electromagnetic radiative losses) without respect to impedance mismatch (since measured CPS lines characteristic impedance is not 50 Ω) and is expressed as:

$$F_{loss} = 10 \times \log(|S_{11}|^2 + |S_{21}|^2). \quad (1)$$

As depicted in Fig. 4, for a 10^{12} p/cm^2 irradiation, a 0.2 dB drop in the loss factor of the 500 µm long line is observed below the Ku frequency band. Such decrease is significantly higher than the measurement accuracy limit due to the variability in the RF probe contact resistance. It is observed that backend metal resistivity is slightly impacted by proton radiation; this variation may suggest a radiation-dependent decrease in silicon substrate resistivity.

Modeling and experimental analysis of active SiGe BiCMOS LNA under electrical RF stress

For this discussion, we use an in-house reliability simulation tool that contains modules of all known degradation mechanism

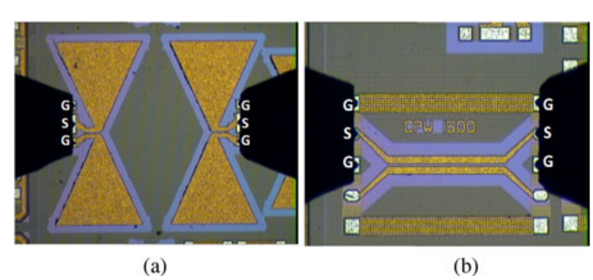

Fig. 3. Photomicrograph of the planar bowtie antenna (a) and the integrated CPS transmission line structures (b).

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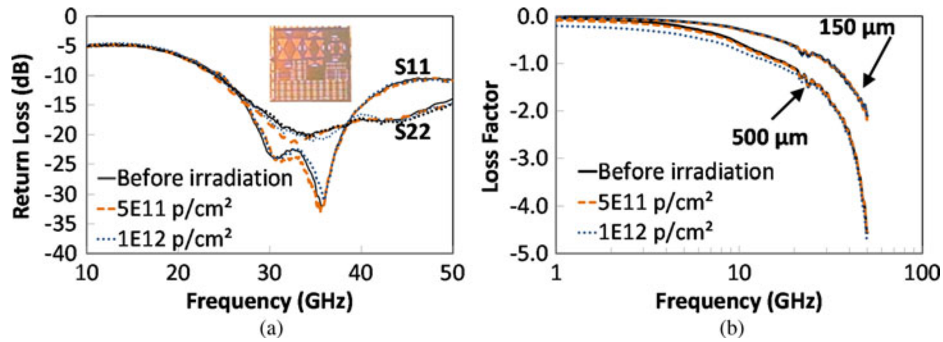

Fig. 4. Return loss of two bowtie slot antennas with various circuitry environments. Inset the photograph of the circuitry. Loss factor measured for two CPW lengths (100 and 500 µm) versus frequency.

models in bipolar and MOS devices. Supported degradation models, based on DC-accelerated stress conditions, are applied to the compact model of transistors introducing parameters shift over time.

The physical degradation phenomena in bipolar devices have been divided into two mechanisms:

- Mixed mode (MM) occurs when the device is simultaneously polarized at very high current and high base-collector bias in order to achieve speed performance [11]. The MM mechanism results in an increase in the base current I_b due to an increase in the interface traps in the emitter–base (EB) spacer and the shallow-trench isolation region.

  The I_b MM degradation model, as a function of stress conditions, is given by (2):

$$\Delta I_b = (A_E + P_E) t_{stress}^{n} e^{\overline{V_{cb\_stress}}^{\,-\alpha}} \left(e^{\left(V_{be\_stress}/((K_B \; T_{stress})/q)\right)} - 1 \right)^{b} \left(e^{V_{be\_read}/(m(K_B \; T_{stress})/q)} - 1 \right) e^{\left(-E_a/(m(K_B \, \Delta T_{read})/q)\right)}, \quad (2)$$

  where: t: aging time; A_e, P_e: effective area and perimeter; n, b and E_a: constants depend on the technology.

  Figure 5 shows simulation results of base current I_b and current gain degradation after MM stress, in function of collector–base stress voltage. The curves show that the degradation of current gain becomes significant from 3.3 V. Simulation results are compared with correspondent degradation model. The curves exhibit a very good matching which attest the reliability simulation tool accuracy.
- Reverse base emitter bias (RVBE) occurs when the EB junction is reverse-biased near breakdown voltages [12]. Also, the RVBE degradation results in an increase in the base current I_b due to interface trap generation at the EB junction perimeter. Equation (3) presents the RVBE DC degradation model:

$$\Delta I_b = P_E \; t_{stress}^{n} e^{\overline{V_{eb\_stress}}^{\,-\alpha}} \left((1-c) + c.e^{\left(-E_a/((K_B \; T_{stress})/q)\right)} \right) \left(e^{\left(V_{be\_read}/(m(K_B \; T_{stress})/q)\right)} - 1 \right) e^{\left(-V_g/(m(K_B \, \Delta T_{read})/q)\right)}, \quad (3)$$

  where: t, aging time; P_e: effective perimeter; V_g: band gap voltage; n, α, and E_a: constants depend on the technology.

To validate the implemented RVBE model in the in-house reliability simulation tool, we also compared the simulated degradation of the base current and the current gain with the model. Simulations are conducted on a SiGe NPN transistor under reverse base–emitter stress voltage. The different curves are shown in Fig. 6. They demonstrate in one hand a very good matching between both, in other words, the accuracy of the tool. On the other hand, we can conclude that the degradation of the gain current becomes significant from −1.7 V.

In reliability simulations, the device or the circuit is simulated in transient mode, and the aging of the modeled parameter, in this case ΔI_b, is integrated over time. Subsequently, this aging is extrapolated to the stress time of interest. Therefore, the circuit could be simulated with the updated parameters.

Same degradation models are considered when the device-under-test is stressed under RF stimuli. The simulator calculates the dynamic (RF) stress damage by summing up the instantaneous damage of the transistor over a short incremental time of a quasi-static stress voltages [13].

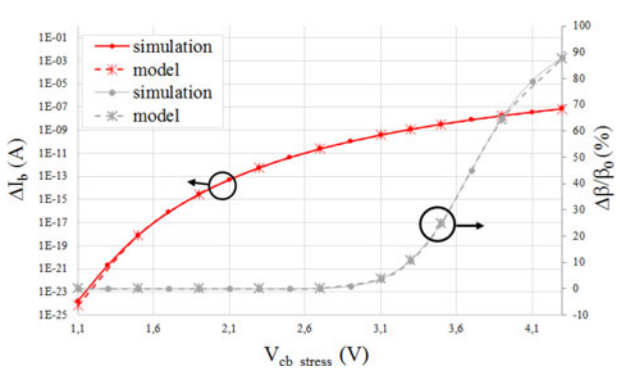

Fig. 5. Comparison of simulated ΔI_b and $\Delta\beta/\beta$ as a function of V_{cb_stress} based on MM degradation model (high-voltage SiGe NPN: after 10 years of stress at 40 °C).

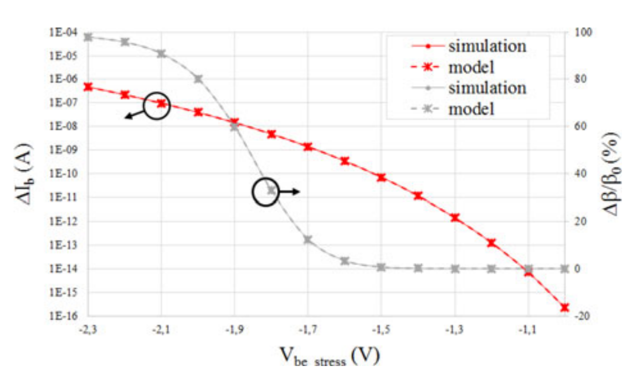

Fig. 6. Comparison of simulated ΔI_b and $\Delta\beta/\beta$ as a function of V_{be_stress} based on RVBE degradation model (high-voltage SiGe NPN: after 10 years of stress at 40 °C).

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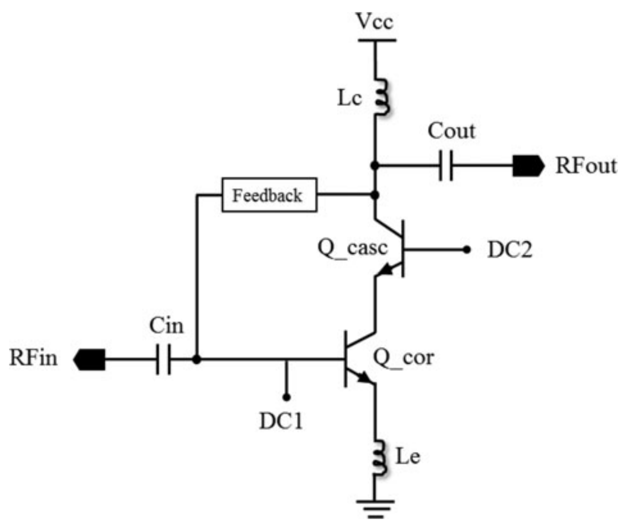

Fig. 7. LNA architecture.

Table 1. Simulated DC biasing evolution during the application of RF power

	RF power OFF	RF power ON
V_{ce_cor} (V)	1.3	0.3
V_{be_cor} (V)	0.752	−0.2
I_c (mA)	9.16	31

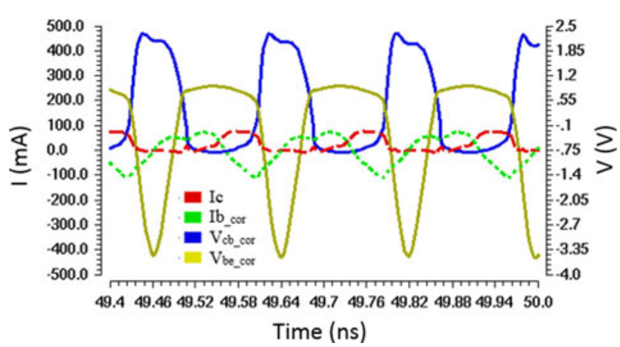

Fig. 8. AC collector–base voltage, AC base–emitter voltage, AC base current, and AC collector current of LNA during the application of RF power stress.

A specific attention is directed toward verifying the applicability of quasi-static-based approximations in using DC stressing data for RF stressing lifetime prediction. In the following, DC and RF stress are applied to LNAs designed for WLAN applications in order to assess the impact of aging on their RF performances. Several reliability studies have been carried out on transistors and circuits under DC stress conditions. The aim of these studies is to identify the physical origin of the degradation mechanisms and provide models describing performance shifts [14,15]. However, the degradation of RF and mill metric circuits under RF stresses remains poorly studied and little-understood subject.

The validation of the quasi-static approximation throughout the comparison between the simulated degradation of the LNA performance, designed in 0.25 µm BiCMOS technology, and measured results permit to develop an improved design methodology, which includes reliability assessment according to the circuit's mission profile.

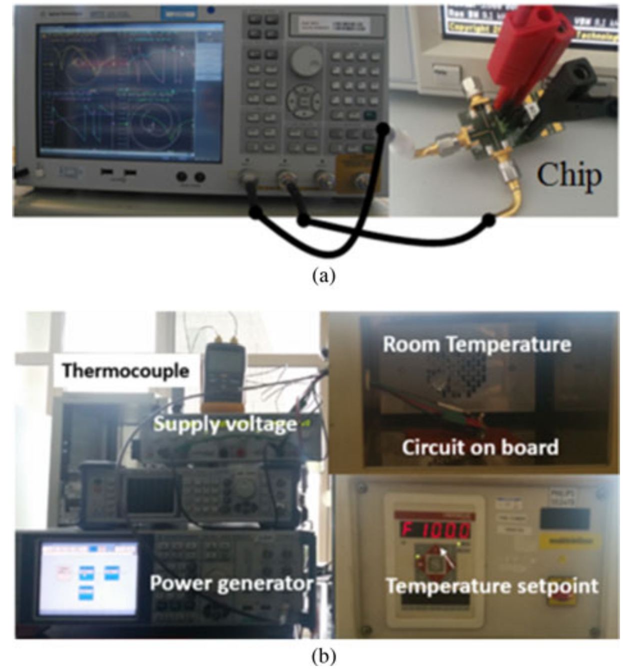

Fig. 9. Set up for RF performance measurement of the fully integrated LNA circuit reported on application board (a) and RF stress application (b).

LNA architecture and specification

The under test LNA is shown in Fig. 7. It consists of a common source configuration using cascode transistors with feedback. This configuration is the most classical topology used in the design of LNAs.

LNA mission profile

The mission profile awareness aids to accurately investigate and validate the design robustness with respect to given requirements. The considered circuit under test operates from 5.15 to 5.85 GHz at a supply voltage V_{cc} of 3.6 V.

The maximum operating temperature is assumed to vary in the range from 85 to 100 °C, and the maximum input power $RF_{in} = 7$ dBm. It is designed for a term of 5 years of operation. Estimated time to failure is defined as the time to reach more than 3 dB gain loss ($\Delta S_{21}/S_{21} > 25\%$). The noise figure (NF) increase is also considered as a failure criterion if it is higher than 3 dB ($\Delta NF/NF > 30\%$). Therefore, reliability simulations are carried out after 5 years of RF stress. Simulation results are compared with the measurements carried out based on the accelerated aging test.

RF-accelerated aging test

In order to accelerate the degradation of the LNA at 5.6 GHz ($V_{cc} = 3.6$ V), we increase the temperature to 100 °C with an input power of 20 dBm. Although at such power level the amplifier compresses, the stress power is still under the power handling capability of the used cascode topology. When the RF stress signal is applied on the circuit, the DC drain current increases from

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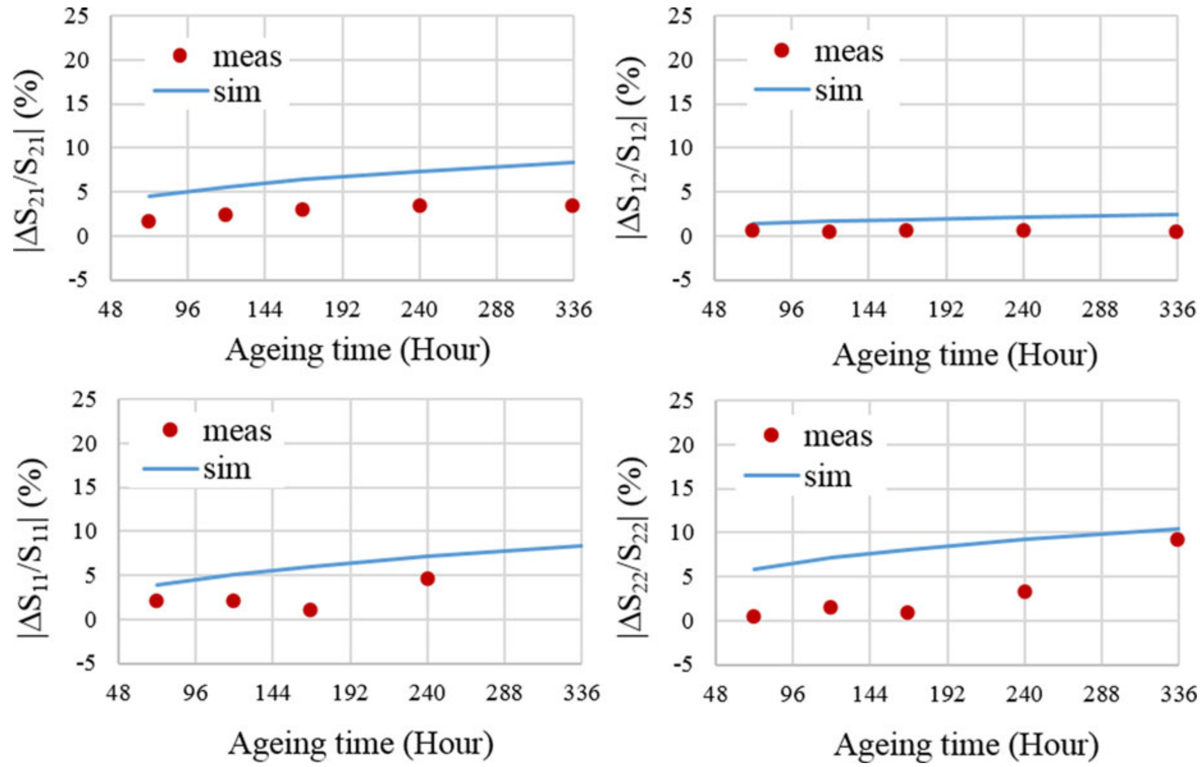

Fig. 10. Comparison between simulated and measured *S*-parameters degradation at 5.6 GHz after 336 h of 20 dBm stress: $\Delta S_{ii}/S_{ii}$ is defined as the relative degradation.

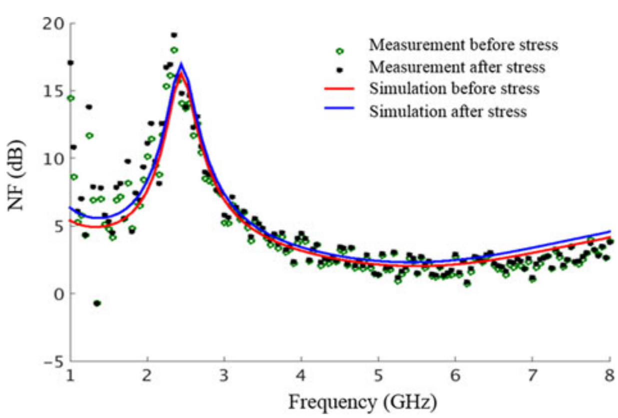

Fig. 11. Comparison between simulated and measured NF after 336 h of 20 dBm stress.

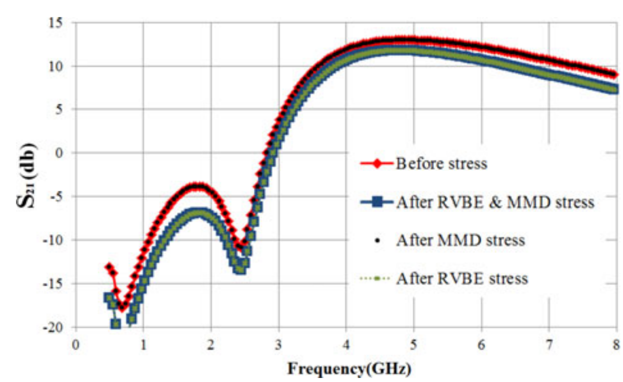

Fig. 12. Simulation of the contribution of MM and RVBE degradation mechanisms to the LNA gain shift after 336 h of 20 dBm stress.

around 9.16 to 31 mA as a consequence of the self-biasing of the LNA circuit. The evolution of the DC biasing during RF stress is presented in Table 1. The RF signals used in the stress are presented in Fig. 7 with a V_{cb} stress voltage peak around 2.5 V and a V_{be} stress voltage peak at −3.8 V.

These peaks exceed the voltage limits of the used technology leading to accelerated degradation under the aforementioned MM and RVBE mechanisms (Fig. 8).

Experimental test-bench description

In order to assess the accuracy of the predictive simulation results, experimental accelerated aging tests are applied on the fully integrated LNA circuit reported on application board, as depicted in Fig. 9.

For fair comparison between simulations and measurements de-embedding procedures are applied for properly taking into account both losses in RF transmission cables and the IC package and board parasitic. All along the stress, the evolution of the RF performances of the LNA are measured in small signal.

The NF and the correlation parameters are measured using a PNA-X instrument in a broad frequency range from 1 to 8 GHz before and after 336 h of stress. The analysis of the reliability results is based on the comparisons between RF performances before and after applying the stress stimuli.

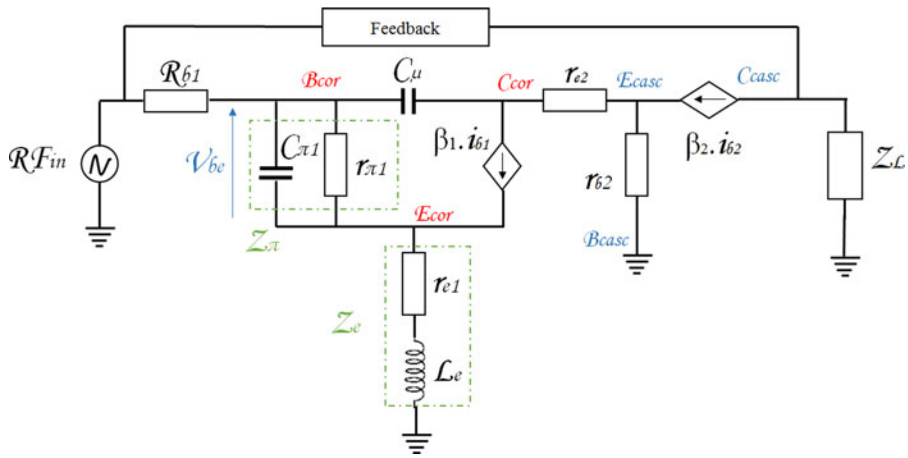

Fig. 13. Small-signal model of cascode LNA with feedback.

Results and discussions

Figure 10 shows the relative variation of simulated and measured S-parameters as a function of aging time. Despite the observed degradation, the circuit did not reach the criterion of failure (in term of S_{21} limits).

As depicted in Fig. 11, the simulated NF increases by 13.5% at 5.6 GHz after stress. Simulated results are compared with the measurements showing good agreement.

In order to identify the mechanism that is mainly determinant of Q_{cor} degradation during RF stress, we apply the following methodology:

- First, we generate the netlist of the aged circuit by activating the two mechanisms RVBE and MM. We then simulate the gain of the LNA described by this netlist.
- Second, we deactivate one of the two mechanisms, for example, RVBE while keeping the MMD mechanism activated, and then

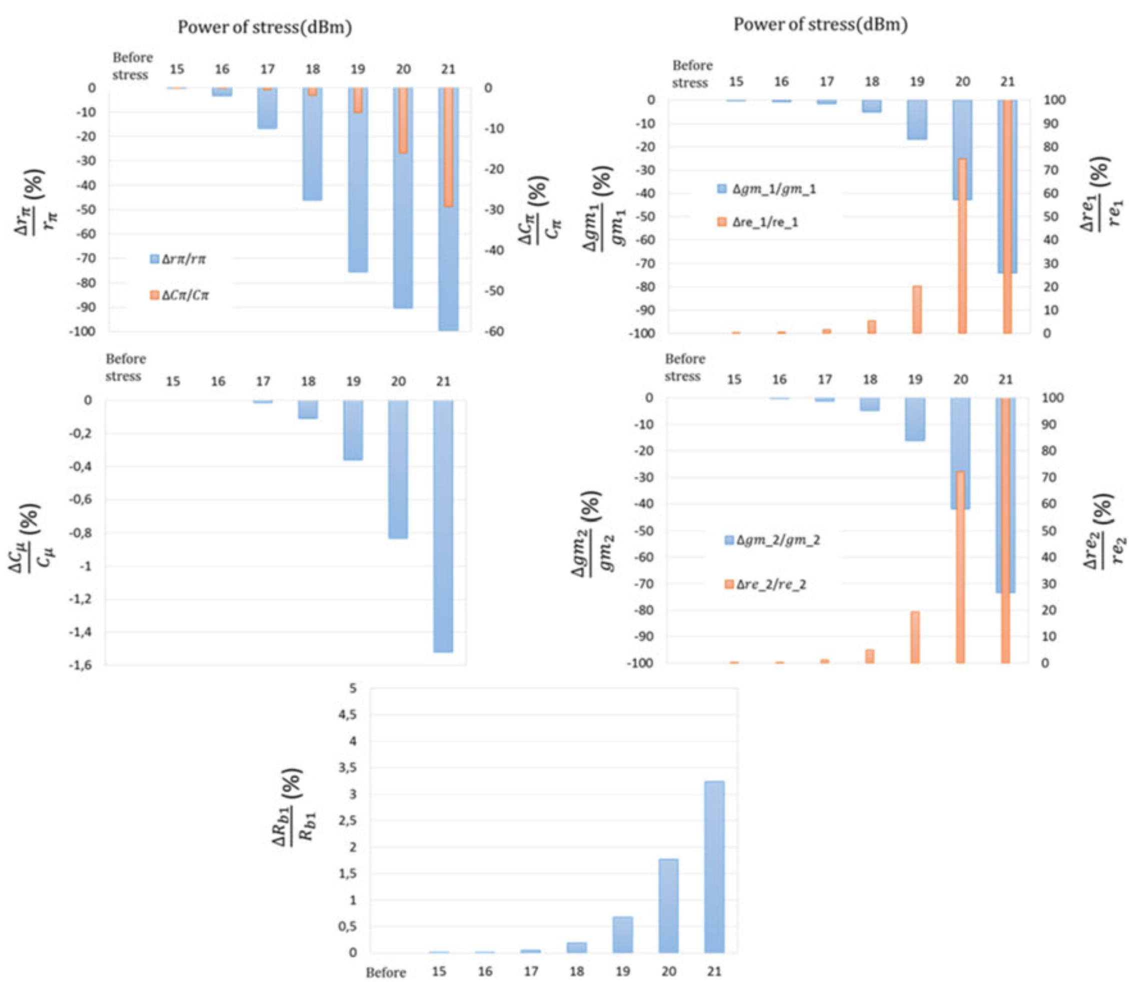

Fig. 14. LNA small-signal parameters degradation after 336 h of stress in function of RF input stress power.

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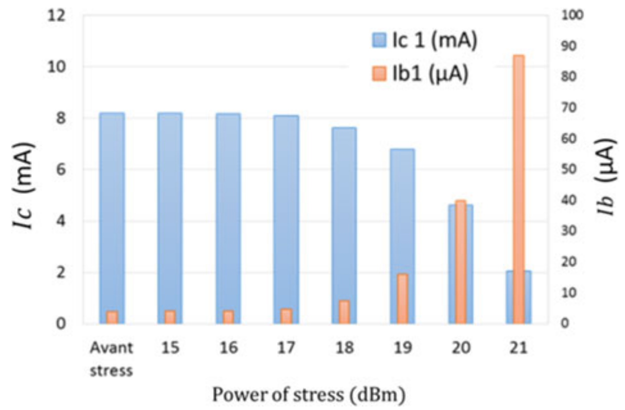

Fig. 15. DC currents after 336 h of stress in the function of RF input stress power.

Table 2. DC power dissipation in function of RF input stress power

RF stress power	DC power dissipation (mW)
Before stress	294 516
15	293 832
16	290 916
17	27 378
18	24 372
19	165 384
20	736 992

we generate the aged netlist to simulate the LNA gain after aging.

- Finally, we redo the same thing by keeping RVBE activated without MMD mechanism.

The simulated gain of these three cases is shown in Fig. 12. As can be seen, the degradation of the LNA is mainly due to the RVBE degradation mechanism. The latter occurs in the presence of a high inverse base–emitter voltage. The MM degradation mechanism has no significant effect on gain shift, because the resulting collector–base voltage is not high enough to trigger it and thus cause degradation.

We are now interested in the variation of the transistors small-signal model parameters (Fig. 13) as a function of the stress RF power. The aim of this study is to determine the sensitivity of the LNA gain to the degradation of these parameters.

We varied the RF power from 15 to 21 dBm @ 5.6 GHz. Then, we extracted the relative degradations of the different small-signal parameters after 336 h of stress.

The studied parameters of the core transistor are: the resistance and the base–emitter capacitance (r_π and c_π), the transconductance g_{m1}, the emitter resistance r_{e1}, and the Miller capacitance C_μ. Concerning the cascode transistor, we focused on its transconductance g_{m2} and its emitter resistance r_{e2}.

The extraction, in relative value ΔX/X, of these different parameters as a function of the stress power is presented in Fig. 14. The negative values correspond to a decrease in the parameter and the positive variation in an increase.

Up to 16 dBm, no degradation is observed on the different parameters. From 19 dBm, degradation begins to be noticeable, then very significant, for a stress power of 21 dBm. Reliability

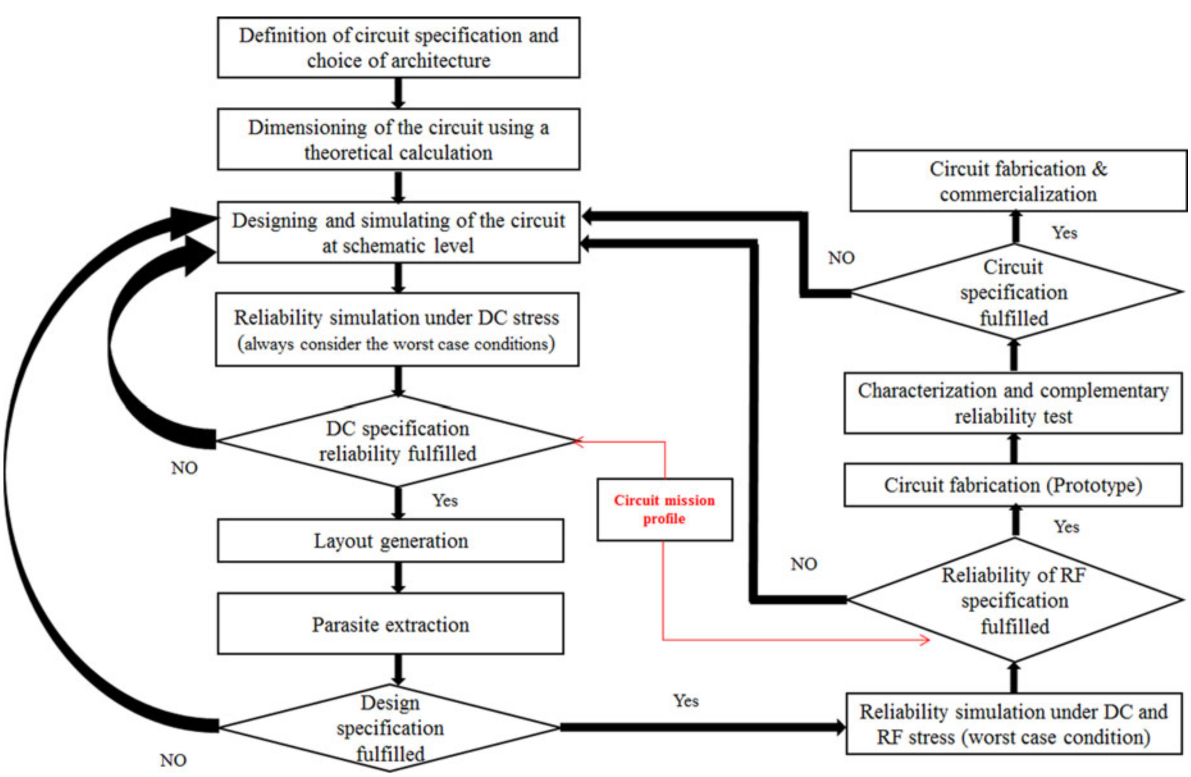

Fig. 16. Design flow aware circuit reliability: design steps illustration including reliability simulation.

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measurement results, presented above in Figs 10 and 11, are conducted under 20 dBm of stress RF power after doing to these simulation analyses.

These simulations show that the transconductances of the two transistors g_{m1} and g_{m2}, extracted at the operating points of the LNA, decreased by 42% at 20 dBm and by 75% at 21 dBm. This represents the main cause of the gain degradation. At 20 dBm, the degradation of r_π, r_{e1}, and r_{e2} reached 90%. However, the degradation of the Miller capacitance C_μ and the basic resistance r_{b1} is insignificant.

These variations in small-signal parameters, mainly due to RVBE mechanism, made the overall degradation of gain and NF.

The source of the LNA noise is mainly the resistance R_{b1}, the current of the base I_b, and therefore the current of the collector I_c of the core transistor.

The increase of the NF is mainly due to the rise of the I_{b1} current and the R_{b1} resistance. Under a stress of 20 dBm, I_b moved from approximately 4 to 40 μA (Fig. 15) and the resistance increases by 1.8% of its initial value (Fig. 14).

The decrease of the drain current after stress leads to DC power dissipation shift. Related simulation results are summarized in Table 2.

Design for reliability

Currently, the design cycle guaranteed only the electrical performance of the integrated circuits before aging. These performances throughout product lifetime are, in general, assured by taking design margins and accelerated aging tests that come in a second complementary phase to guarantee the circuit reliability. In case of degradation, a reactive design correction is launched. This will necessarily mean a delay in placing the product on the market. To avoid this inconvenience, we propose a general design flow, which takes into account the circuit reliability improvement (Fig.16).

Thanks to the use of reliability simulation tool, great improvement in terms of performance and reliability trade-off could be achieved. In fact, without such tool designers are obliged to take margins on design parameters according to the technology being used. To conclude, this design aware circuit reliability will be very helpful in ensuring first-time-right success target with reduced time-to-market.

Conclusion

In this paper, the impact of extreme environmental conditions on SiGe:C BiCMOS-integrated circuits is experimentally studied in the perspectives of qualifying silicon-based technology for space applications. Canonical representative structures including linear (passive interconnects/antennas) and non-linear (LNAs) are used as carriers for assessing the impact of aggressive stress conditions on their RF performances.

Predictive modeling of degradation effects using in-house tooling solution is compared with the experiments demonstrating good agreement. Ongoing work concerns the analysis of interaction mechanisms (substrate resistivity variations, couplings/interferences, and drift in DC and RF characteristics) as a function of temperature and stress power levels for assessing mission-critical profiles for emerging RF and mm-wave applications.

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Sidina Wane holds a Dr.-Ing.-HDR degree in electronic circuits and systems working on chip-package-PCB co-design, co-simulation, and experimental co-verification. His main interest is in the field of power integrity, signal integrity, EMC (electromagnetic compatibility) and EMI (electromagnetic interference) in integrated circuits/systems for RF (radio frequency), mm-wave, and THz applications. In 2013, he received the HDR (Habilitation à Diriger des Recherches) diploma on the topic of "Power

Integrity, Signal Integrity, EMI & EMC in Integrated Circuits and Systems: Towards Multi-Physics Energy-Oriented Approaches." The distinguished awards bestowed on him include the Leopold Escande award together with the GEET (Génie Electrique Electronique et Télécommunications) award for his Ph.D. dissertation in 2002, the innovation award presented by the French ministry of research in 2003. He is member of the European Management Committee for COST Action 1407 relative to stochastic radiations of densely integrated circuits for emerging 5G and Internet-Of-Things systems. He is member of the French IEEE sections on Instrumentation and Microwave Theory and Techniques. He has several European and US patents on technological implementation of RF and mm-wave circuits and systems. Dr. Wane is the architect of TWF (transverse waves formulation) – a full-wave electromagnetic solver based on energy considerations suitable for RFICs (radio frequency integrated circuits) and module-based co-design and co-simulation. Dr. Wane is the founder and CEO of eV-Technologies – a high-technology company providing leading edge energy-aware tools, instrumentations and chip-package-PCB-antenna co-design solutions for RF, millimeter-waves and optical applications based on semiconductor manufacturers in Europe with partners across the world. eV-Technologies offer unified EDA & Instrumentation approach built around a comprehensive measurement platform for broadband characterization, validation and test of components, circuits and systems with loop-back to modeling and failure analysis.

Aziz Doukkali received his Ph.D. in Electronics in 1990 from the University of Montpellier (USTL). He started with CRISMAT Laboratory until 2000 to develop superconducting materials for microelectronics. From 2000 to 2008, he worked in failure analysis field in LaMIPS Laboratory. Since 2008, he has been working on BIST activities and IC reliability.

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Rosine Coq Germanicus was born in Schoelcher, Martinique, France. She received her Ph.D. degree in 2002 from the University of Montpellier 2 (France) with CNES and ALCATEL SPACE in radiation effects on optoelectronics device for space reliability. Since 2003, she is an Associate Professor at the University of Caen (IUT-CRISMAT). Her research interests include radiation effect for devices space qualification and near field probe microscopy with particular emphasis on local electrical characterizations of semiconductor devices for micro and nano-electronics reliability in high integrated process.

Françoise Bezerra received her degree in Electronic Engineering from the French Civil Aviation National School in 1991. She joined the CNES, the French Space Agency, in 1992 as a quality insurance engineer in charge of microprocessors, ASICs and FPGAs. Since 2008, she is Principal Investigator of the CARMEN/MEX instrument that studies radiation effects on electronic devices on board of JASON2, SAC-D, and JASON3 satellites. Finally, she is a Radiation Safety Officer for the CNES Toulouse and is involved in the local Radiation Protection Community (Vice-President of the RAMIP Association). Françoise BEZERRA has co-authored more than 70 papers in radiation testing or in-flight experiments and has also chaired various sessions at RADECS conferences. In 2017, she entered the RADECS Association Council Board, in charge of workshops. She will be the RADECS 2019 conference technical chair.

Guy Rolland received the Engineers degree in Electronics in 1977. In 1978, he was with the Physic-Electronic Department, CNES (the French Space Agency), Toulouse, France. Until 1988, he was responsible for the CCD characterization laboratory and for the theoretical modeling of optoelectronic components. He was involved in numerous earth observation and scientific projects. From 1989 to 1997, he was particularly involved in process and device simulations applied to optoelectronics. He is today responsible for researches in the field of space radiation environment modeling and the effect of radiation on optoelectronic components.

Patrick Martin received the B.E. and M.E. degrees from Caen University and Ph.D. from Rouen University, France, in 1981, 1983, and 1991, respectively. His first areas of research interest were the development of data flow architectures and algorithms for real-time inspection by computer vision-assisted automatic control of quality in industrial process. He joined the LaMIPS Ensicaen, in 2004, since he works on robustness, reliability, and instrumentation for reliability of electronic devices.

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Guillaume Boguszewski is the founder and CEO of CYleone. He earned a PhD in electronic & electro-magnetism from INP-Polytech, Bordeaux for embedded systems (SiP, SoC, etc.). He obtained Master of Physical Sciences from Montpellier University. His professional experience for the last 15 years include: Philips-NXP Semiconductors (Deutchland, Germany, France); NASA ECE Lab (Tucson/Phoenix, AZ, USA); Domestic National Security; and Data management (data analysis, data system engineering, and data vizualization).

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