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Application of Electron Holography to Semiconductor Structures and Devices

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Scaling of semiconductor devices allows one to improve device speed and increase chip complexity. However, short-channel effects [1], i.e. decrease of threshold voltage at which device turns on and off, degrade once device size decreases. Shallow and abrupt (ultimately diffusionless) p-n junctions allow one to control short-channel effects and continue scaling. We will present results on how dopant diffusion during formation of p-n junctions can be controlled and characterized by electron holography.

Mechanical stress provides an effective “knob” to improve device performance. In particular, tensile stress increases electron mobility in the channel of the device while compressive stress increases hole mobility. One of the ways to provide tensile stress in the channel of n-FET device is to place Si:C in areas adjacent to channel. We will discuss measurement of mean inner potential in intrinsic Si:C, which necessary prior to analysis of p-n junctions. Finally, using combination of SIMS, XRD and electron holography we will provide insight into electrical activity of Carbon in Si:C and dopants in p-n junctions in structures with Si:C.

References

[1] 1. L. D. Yau, *Solid-State Electronics,* vol. 17, pp. 1059, 1974