# Design and modeling of an ultra-wideband low-noise distributed amplifier in InP DHBT technology

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## Abstract

This paper reports on an ultra-wideband low-noise distributed amplifier (LNDA) in a transferred-substrate InP double heterojunction bipolar transistor (DHBT) technology which exhibits a uniform low-noise characteristic over a large frequency range. To obtain very high bandwidth, a distributed architecture has been chosen with cascode unit gain cells. Each unit cell consists of two cascode-connected transistors with 500 nm emitter length and $f_t/f_{max}$ of ~360/492 GHz, respectively. Due to optimum line-impedance matching, low common-base transistor capacitance, and low collector-current operation, the circuit exhibits a low-noise figure (NF) over a broad frequency range. A 3-dB bandwidth from 40 to 185 GHz is measured, with an NF of 8 dB within the frequency range between 75 and 105 GHz. Moreover, this circuit demonstrates the widest 3-dB bandwidth operation among all reported single-stage amplifiers with a cascode configuration. Additionally, this work has proposed that the noise sources of the InP DHBTs are largely uncorrelated. As a result, a reliable prediction can be done for the NF of ultra-wideband circuits beyond the frequency range of the measurement equipment.

## Introduction

Low-noise ultra-wideband amplifiers (low-noise distributed amplifier, LNDA) are not very common, but they are key components in several mm-wave and THz applications such as high-resolution radar, material spectroscopy, imaging systems, and fiber optic receivers. The frequencies of interest lie in the range of W-band (75–110 GHz), D-band (110–170 GHz), and G-band (140–220 GHz). As transistor speed has been increasing, with record performance exceeding 1 THz $f_{max}$ [1–5], one can now realize integrated circuits in the terahertz frequency range (0.3–3 THz). Reports have been published on power amplifiers beyond 1 THz [6] for InP HEMT and 0.6 THz for InP HBT technology [7, 8]. The wide bandgap in the InP collector of an InP HBT provides a higher breakdown voltage as compared with HEMT devices. This feature makes it an attractive choice for high power sub-THz and terahertz amplifiers.

With respect to ultra-wideband LNDA, several publications can be found in the literature with bandwidths larger than the octave range: SiGe HBT [9], GaAs mHEMT [10], InP HBT [11], and CMOS [12]. Several challenges exist in designing such ultra-wideband amplifiers, such as finding suitable topologies to achieve uniform forward gain response for the full band and a low-noise figure (NF) over this bandwidth, simultaneously. Another major challenge is to measure NF beyond 100 GHz and predict its behavior beyond this frequency.

In order to achieve wideband gain beyond the octave bandwidth, the distributed architecture is the most promising solution [13]. Up to 235 GHz of bandwidth [14] have been reported. In this topology, the loss of an artificial microstrip transmission line is compensated by the gain cell, arranged periodically over the line. Using proper inter-stage line impedances, unit cell and termination resistance, uniform gain characteristics can be achieved. Although this type of amplifiers is not ideal for ultra-low-noise purposes, it solves the aforementioned challenges simultaneously. This work outlines the design and modeling of a distributed amplifier with the desired properties of both gain flatness and low-noise operation. A bandwidth of 40–185 GHz is achieved with an NF of 8 dB over a measured frequency range from 75 to 105 GHz. This paper is an extension of the paper published in [15]. The extensions comprise a large-signal model of the transistor, as well as a noise model. The former is applied in the optimization of the circuit for finding the best bias condition for the transistors. Furthermore, in distributed amplifiers there exist a trade-off between gain flatness and saturated output power which can only be assessed by a large-signal model. The latter is indispensable in explaining the noise measurements and predicting the NF outside the frequency range covered by the noise characterization set-up, particularly above its maximum frequency.

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The organization of the paper is as follows: Section "InP DHBT process" presents the technology of the InP DHBT process and is followed by the transistor modeling in the section "Transistor modeling." In the section "Noise modeling," the NF predictive model is explained. In the section "Circuit design," the circuit design is presented and the NF behavior versus frequency is predicted using the uncorrelated noise model. In the section "Measurements and discussion," the measurement results are reported, covering small signal *S*-parameters, and NF. Finally, the section "Conclusions" presents the conclusions and the future work.

## Technology

### InP DHBT process

The circuit presented in this paper is based on the FBH transferred-substrate InP-DHBT technology, as illustrated in Fig. 1. The base-line process contains single and double finger InP/InGaAs DHBTs with 800 nm emitter widths [16]. Three layers of electroplated gold embedded in BCB are used as interconnects, ground plane, and microstrip lines, MIM capacitors with a capacitance of 0.3 fF/μm² and NiCr thin film resistors with a sheet resistance on 25 Ω/sq. are used as passive elements. A high-resistivity silicon substrate with prefabricated through-silicon vias was used as host wafer in the wafer bonding process, which can be substituted with a fully processed BiCMOS wafer [16]. As a recent development down-scaled devices with 500 nm emitter widths and an optimized layout cell have become available. A single finger $0.5 \times 6$ μm² InP/InGaAs DHBT biased at $V_{CE} = 1.5$ V exhibits $f_t/f_{max}$ values around 360/492 GHz, respectively, at a collector current density of 3.6 mA/μm². The circuit presented in this paper is based on transistors with 500 nm emitter width.

### Transistor modeling

The large-signal model topology proposed for the down-scaled transferred-substrate InP DHBT device is shown in Fig. 2. The FBH's custom HBT model forms the inner core of the large-signal model topology. Despite the fact that the FBH HBT model was originally developed for GaAs HBT devices (having a single base-emitter heterojunction) it has proven to be versatile enough to describe also DHBTs in the InP/InGaAs material system [17]. To extend the validity of the model structure toward higher millimeter-wave and THz frequencies, the model is embedded by an external network describing parasitic effects associated with via transitions and device electrodes within the layout cell itself [18]. In this approach the elements of the external parasitic network are determined using full 3D electromagnetic (EM) simulation and include the skin-effect in the conductors and ultra-thin SiN$_x$ passivation layers in the stackup. The external parasitic network can be identified considering the EM simulation results from two structures only; (1) an open structure with the active layers of the InP DHBT removed and (2) a short structure in which the collector and emitter metallization are connected together. The EM simulation is performed to 325 GHz to accurately capture distributed high-frequency effects. The EM simulated results for the short structure is used to model the frequency dependent inductance and resistance of via transitions and device electrodes. The frequency dispersion in the extracted open structure capacitances versus frequency can be used to distribute the external network elements along the external device structure. The EM simulation assisted parameter extraction

approach has the advantage over a purely measurement based approach that a significantly more complicated external network can be identified. This is because the EM simulation results are not corrupted by unwanted measurement artifacts such as probe-to-probe coupling, multimode propagation, and radiation associated with on-wafer characterization of small-size devices. Having identified the external parasitic network structure it can be used to embed the existing FBH HBT model structure for the InP DHBT devices. For convenience, the innermost reactive parasitic elements are absorbed into the FBH HBT model as shown in Fig. 2.

Following the extraction of the extrinsic parasitic network, the FBH HBT model parameters are determined based on measured multi-bias *S*-parameters and DC characteristics. The *S*-parameters used for extraction were corrected using on-wafer multi-line through-reflect-line (TRL) calibration setting the reference plane for model extraction at the boundary of the layout cell. Further de-embedding of the external parasitic network leads to an active device structure consistent with standard small-signal extraction techniques for HBTs [18]. Figure 3 compares the multi-line TRL corrected *S*-parameters, measured from 50 MHz to 110 GHz, to the model response for bias points $V_{ce} = 1.5$ V, $I_c = 0.9$ mA, 5.4 mA, 9.6 mA, and 14.1 mA. In general, the proposed large-signal model structure is able to describe the measured data very well. The model response neglecting the external parasitic network is also shown in Fig. 3 using black dots. In general, the accuracy of the model suffers significantly above ~40 GHz. Of course, a traditional measurement based parameter extraction approach may absorb the external parasitic network elements into the FBH HBT large-signal model structure and the deviation between the modeled response and the measurements may not be as significant as shown in Fig. 3 (see [17] for an example using $0.8 \times 5.6$ μm² InP DHBTs). It is however important to stress that such a modeling approach is fundamentally incorrect and the lack of distribution of the parasitic elements along via transitions and device electrodes will limit the validity of the model at higher frequencies.

## Noise modeling

Predicting the noise performance of a circuit requires noise models describing the noise sources present in the circuit. Besides all resistances exhibiting thermal noise, a proper description of the shot noise at the HBTs pn junctions is required. Since the shot-noise power is directly linked to the DC current and the chip temperature controls the thermal noise, noise modeling remains tedious only for the following two reasons: the high frequencies require highly accurate modeling of distributed effects, and the correlation between the shot-noise sources needs to be known very well. The first issue is not specific to noise, and it is taken care of as discussed in the previous sections on HBT modeling and circuit design. The second issue is related to the question of how close the noise of the base-collector junction is correlated with the noise originating in the base-emitter junction.

Shot noise sources are commonly implemented as shown in Fig. 4 [19]. The model assumes that the shot noise at both junctions originates basically from the same current and can therefore be considered to be correlated [19, 20]. The correlation is linked to the base-collector transport time and can be described by an equivalent noise correlation time delay $\tau_n$. This time constant can vary between a fraction of the base-collector transit time $\tau_{bc}$ down to $\omega\tau_n \approx 0$, which is a common assumption implemented in traditional large-signal noise models since it is very easy to code [19].
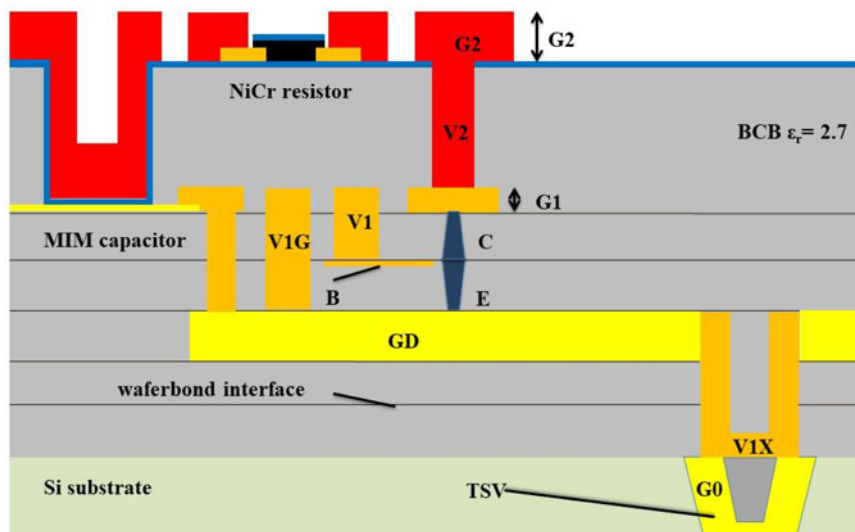
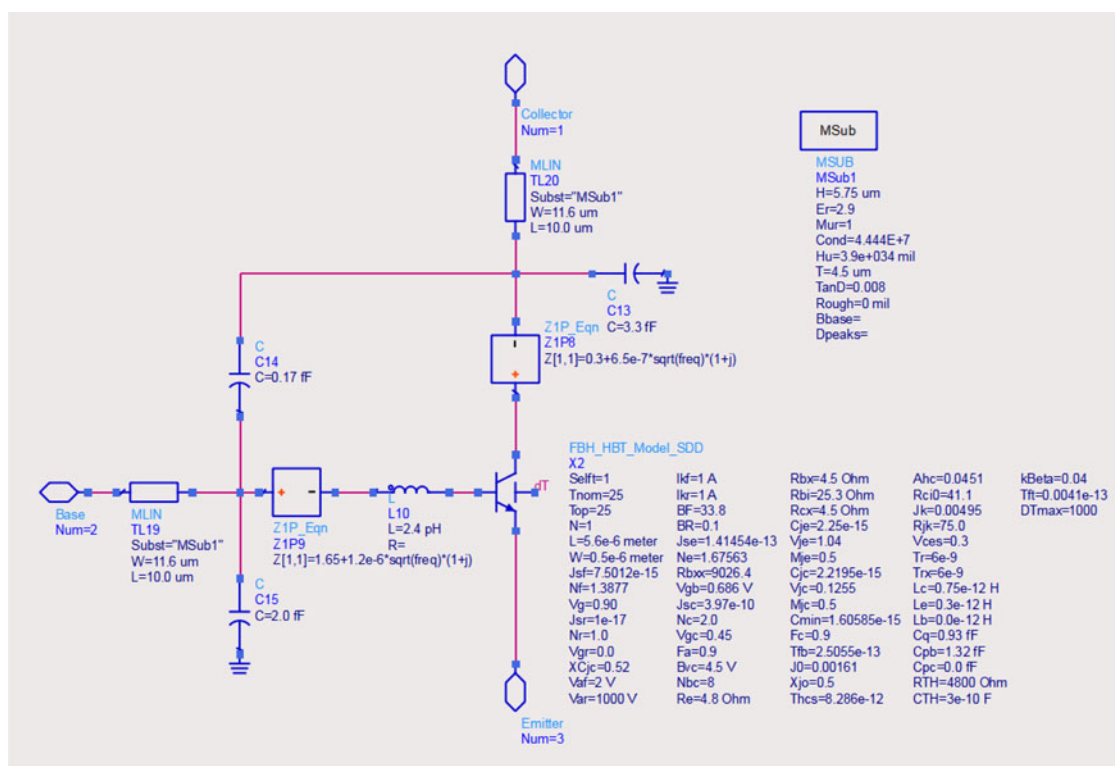**Fig. 1.** Layer stack of transferred-substrate (TS) process.



**Fig. 2.** Large-signal model structure for 0.5 × 5.6 µm² transferred-substrate InP DHBT.

The only degree of freedom in the noise modeling therefore is the noise correlation time constant $\tau_n$, which requires to be determined from measurement. For III-V HBTs, we found $\tau_n$ to almost equal time-delay $\tau_{bc}$ of a InGaP/GaAs HBT operating at L-band [21], but to decrease to a small fraction of $\tau_{bc}$ with shrinking layer thickness and increasing cut-off frequencies for these devices [22]. For the transferred-substrate DHBT technology used in this work, noise parameters were measured up to 26 GHz in order to investigate the noise properties, especially regarding $\tau_n$. It was found that $\tau_n$ close to the base-collector transit time yields lower minimum NFs toward higher frequencies compared with the approximation $\omega\tau_n \approx 0$ which is predicting a steeper slope [23].

In the course of this work, 50-Ω NF (NF$_{50}$) was measured in the frequency range of 75–105 GHz in order to validate the model's extrapolation capability. Figure 5 shows the measurement together with NF$_{50}$s calculated from the measured noise parameters up to 26 GHz reported in [23] (bullets) compared with simulated values (lines). The device under test was a single-finger transfer-substrate InP DHBTs with an emitter area of $0.8 \times 6$ µm² measured at the same bias points as used in the design of the circuit. The simulations reveal the impact of the noise correlation time constant on the actual NF around 100 GHz. As expected from our previous work, the predicted slope of NF$_{50}$ increases with decreasing $\tau_n$. Apparently, higher $\tau_n$ allow the noise
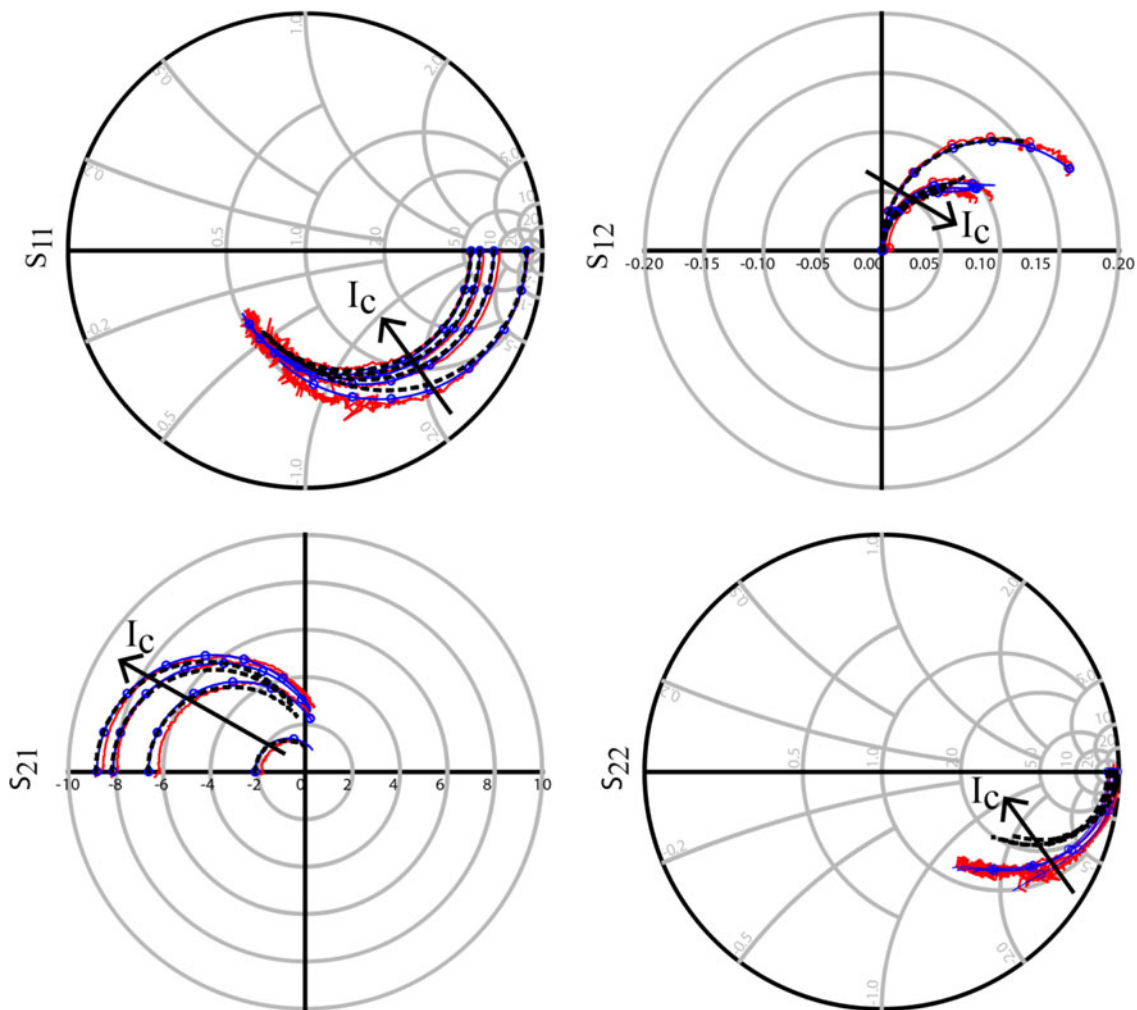
**Fig. 3.** Measured (red solid lines) and modeled (blue solid lines with circles) *S*-parameters from 50 MHz to 110 GHz at the bias points: $V_{ce}$ = 1.5 V at $I_c$ = 0.9, 5.4, 9.6, and 14.1 mA.

contribution of the two pn-junctions to cancel out as frequency increases. The figure shows three possible model assumptions: the dashed line corresponds to $\tau_n = \tau_{bc}$, and the dashed line corresponds to $\omega\tau_n \approx 0$. The dash-dotted line in between was simulated assuming $\tau_n = 0.25\ \tau_{bc}$. The measurement beyond 26 GHz, however, was performed together with the measurement of the amplifier, as discussed below. For the design, the noise model was used to extrapolate the noise behavior beyond 26 GHz assuming $\omega\tau_n \approx 0$. It was not only in line with the 26 GHz-measurement, but also easily coded into the model since it did not require any estimate of transit times. And even though this assumption is underestimating $\tau_n$ which would be in the range of $0 < \tau_n < 0.25\tau_{bc}$ by lightly more than 0.5 dB at 50 $\Omega$, we consider the model very well suited in practical circuit design where it might be advantageous to be on the safe side.

## Circuit design

To achieve ultra-wideband gain characteristics and low noise throughout the bandwidth, a distributed architecture with five unit cells is chosen, as shown in Fig. 6. The unit cells comprise two single-finger $0.5 \times 6\ \mu m^2$ transistors arranged in a cascode configuration [15].

The cascode configuration improves the gain-bandwidth product (GBP) by reducing the Miller effect. As a result, the input capacitance is lowered and input-to-output isolation is boosted. Several approaches have been taken to improve the GBP, among which introducing a small inductance in the form of a transmission line, $L_e$, helps to increase the gain at higher frequencies. The optimum value of $L_e$ = 20 $\mu$m for each unit cell was determined by studying gain and stability factor as a function of frequency, as shown in Fig. 7. The artificial transmission lines $L_a$ and $L_b$ are chosen such that the maximum gain-bandwidth is achieved. Since the transistor is matched differently at input and output, the line segments, $L_a$ and $L_b$, have widths of 22 and 7 $\mu$m, respectively.

To obtain high gain, the transistor, $T_{ce}$, is arranged in the common-emitter configuration without source degeneration. This improves the overall gain of the transistor in exchange of gain flatness. Since the $f_t/f_{max}$ values of the 500 nm transistor are ~360/492 GHz, respectively, the circuit gain performance deteriorates around 185 GHz. In order to obtain flat gain characteristic with stable operation, a small inductance in the form of a transmission line, $L_{cb}$ of length of 120 $\mu$m, is introduced between the transistor, $T_{cb}$, and the upper transmission line, $L_a$. This optimum value has been found by simulating the forward gain and *k*-factor of each cell and varying $L_{cb}$, as illustrated in Fig. 8.
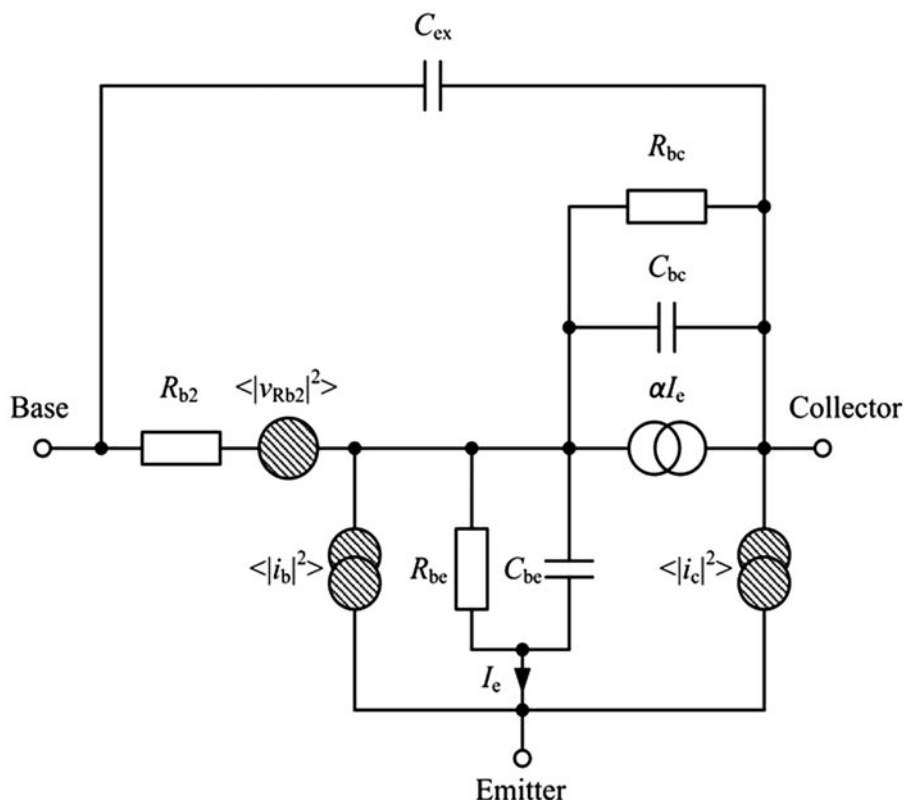
**Fig. 4.** Equivalent circuit of the intrinsic HBT including shot-noise sources and thermal noise source of the intrinsic base resistance.
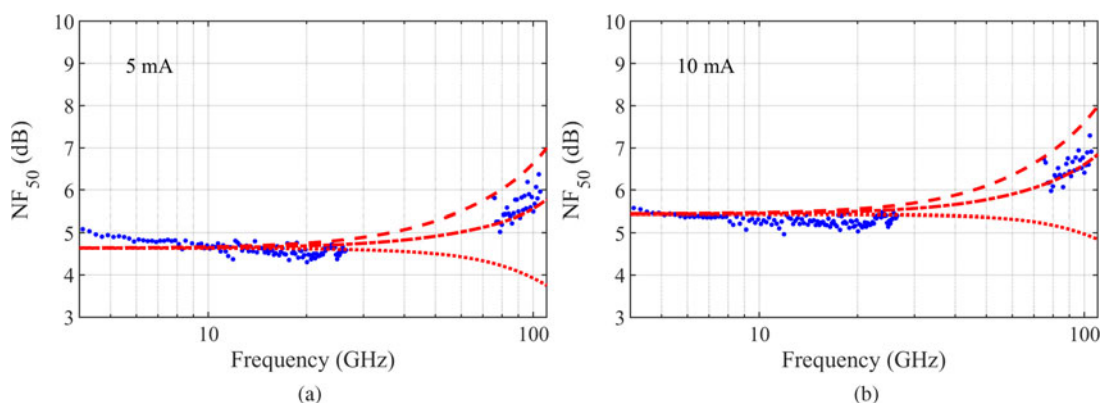


**Fig. 5.** Measured (bullets) and simulated $NF_{50}$ of a single-finger InP DHBT at (a) $I_c = 5$ mA and (b) $I_c = 10$ mA at $V_{ce} = 1.5$ V. Dotted line: simulation assuming that $\tau_n$ equals of the base-collector time delay, dash-dotted line: a quarter of total time delay, and dashed line assuming $\omega\tau_n \approx 0$.

In a cascode configuration, the capacitor $C_b$ of the common-base transistor $T_{cb}$ can be tuned for optimum gain and output power. When increasing the value of $C_b$, the gain flatness at higher frequencies is improved, at the expense of saturated output power. From simulations, an optimum value of 400 fF is chosen as the best compromise between bandwidth and output power. The termination resistances, $R_{term1}$ and $R_{term2}$, are chosen as 30 and 20 $\Omega$, respectively, providing the best input and output reflection match. Finally, matching stubs, $L_{stub1}$ and $L_{stub2}$ of lengths 50 and 75 $\mu$m, respectively, were used to further improve input and output matching. An input matched line $L_m$ of length 200 $\mu$m additionally enhances input matching for the frequency band from 40 to 185 GHz. After all the adjustments for gain-flatness and GBP improvement, the resulting NF is plotted against frequency, as presented in Fig. 9(a). The simulated NF indicates a fairly uniform behavior over the frequency range

with a value less than 10 dB up to 150 GHz. A photograph of the circuit is provided in Fig. 9(b).

## Measurements and discussion

### Small signal measurements

Small-signal measurements were performed using off wafer calibration for DC-140 GHz and on-wafer calibration for 140–220 GHz using 50 $\mu$m pitch GSG probes in both cases. The measured $S$-parameters are plotted against the simulation data in Fig. 10. Using the model parameters as obtained from the section "Transistor modeling," there is very close agreement between simulation and measurement. The small difference at the highest frequency range is due to process variation which leads to higher attenuation of the transmission lines beyond 150 GHz.
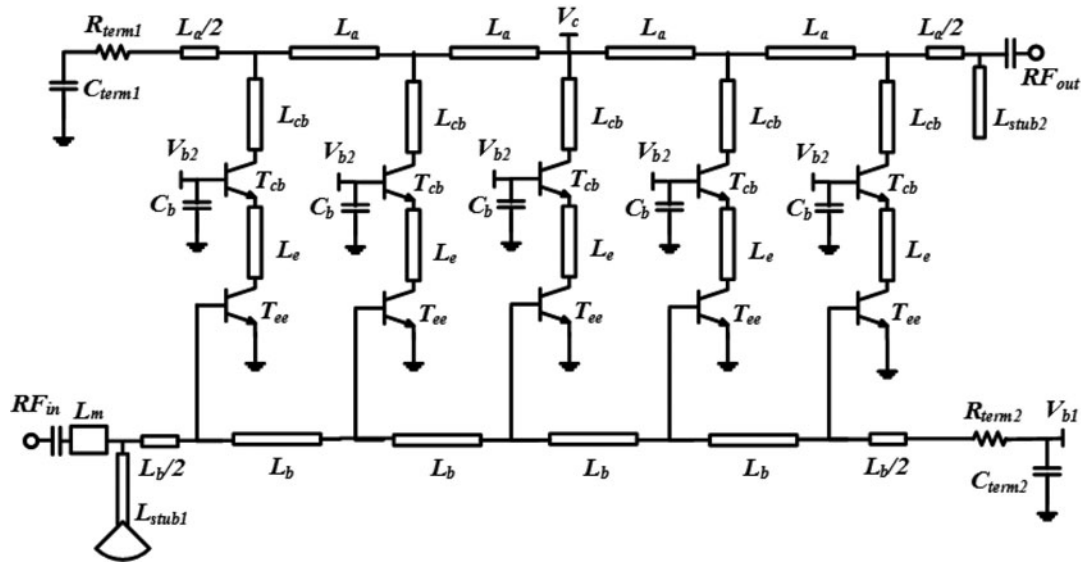
**Fig. 6.** Simplified circuit schematic ($V_{b1}$, $V_{b2}$, and $V_c$ are the DC bias for the circuit).
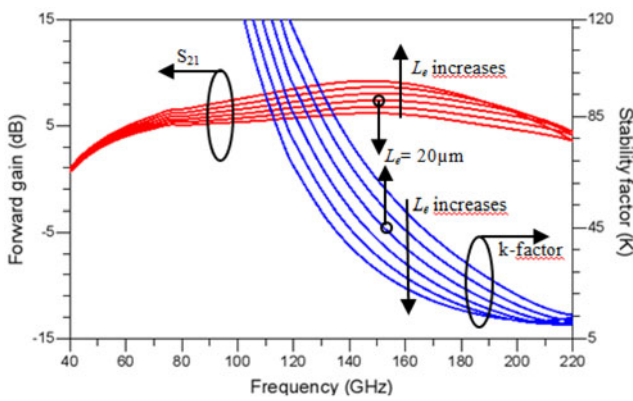


**Fig. 7.** Simulated $S_{21}$ and stability factor of a cell versus frequency, varying line length $L_e$ from 0 to 50 μm [15].
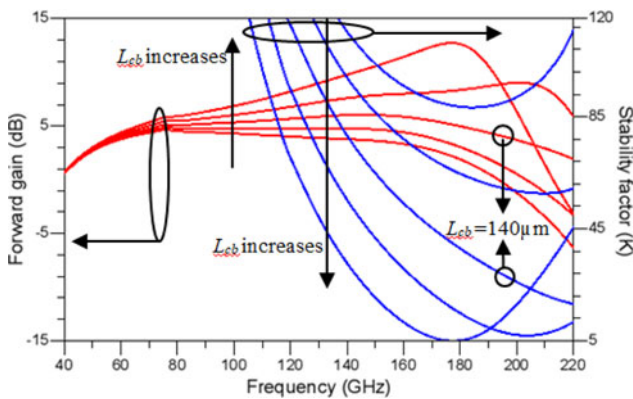


**Fig. 8.** Simulated forward gain ($S_{21}$) and stability factor of each cell versus frequency, varying line length $L_{cb}$ from 40 to 200 μm [15].

The forward gain, $S_{21}$, is relatively flat with an average value of 10 dB with a variation of only ±1.5 dB from 40 to 185 GHz. This flatness is the result of the appropriate choice of gain peaking inductances as discussed in the previous section. In the simulation

of $S_{21}$, a peaking is observed at 185 GHz which comes from a too low line loss prediction at high frequencies. This is absent in the measurements where the real line losses are high enough to suppress this effect.

The cut-off frequency of the input transmission line with input capacitance plays an important role regarding the upper limit of the BW (up to 185 GHz). The cut-off frequency of the input lines in around 200 GHz which is lower than $0.5 \times f_{max}$ of the transistors. Therefore, the circuit is currently limited in BW by the input transmission line. The reflection parameters, $S_{11}$ and $S_{22}$, are both around −10 dB in the range 60–170 GHz. For the remaining operating range of 40–60 GHz and 170–185 GHz, the matching is below −5 dB. There is a peaking at low frequencies around 7 GHz, as can be seen from Fig. 10. This is due to insufficient decoupling from the DC-sources during measurements. The $k$-factor exceeds 3.5 at these frequencies, as can be seen in Fig. 10(b), which proves that the peaking is not caused by oscillations from the circuit. The circuit has a minimum $k$-factor of 2.2 at 190 GHz, indicating stable operation throughout the entire frequency range. The total DC power consumption was approximately 96 mW.

### Noise figure measurement setup

The on-wafer noise measurements were performed at Fraunhofer Institute IAF in Freiburg, Germany. The setup shown in Fig. 11 comprises a commercial mixer module, whose local oscillator input is driven by a multiplied synthesizer signal. The NF analyzer controls the synthesizer as well as the noise source and evaluates the down-converted signals. A similar measurement setup for NF measurements in the D-band has been reported in [24].

### Measured data and comparison with simulations

An essential feature for the successful design of an ultra-wideband LNDA is the underlying noise model for the transistors. These models are usually based on the measurement of the four noise parameters using a source-pull setup, which usually is limited to rather low frequencies up to 26 or 105 GHz at best. The design
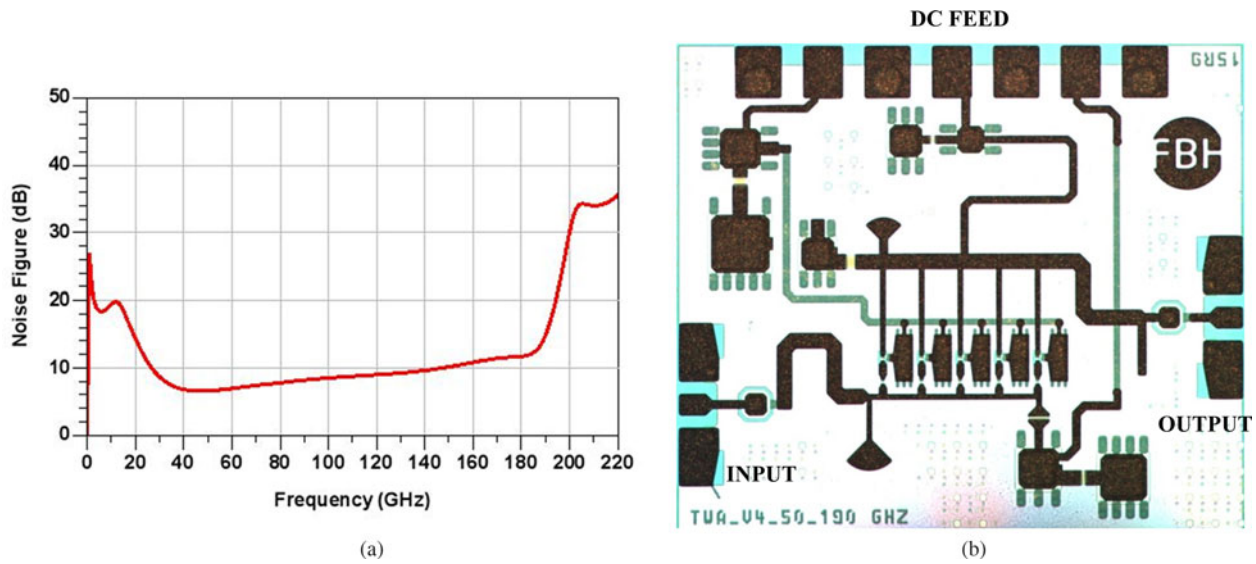
Fig. 9. (a) Simulated NF of circuit versus frequency. (b) Photograph of the distributed amplifier (0.8 × 0.75 mm²) [15].
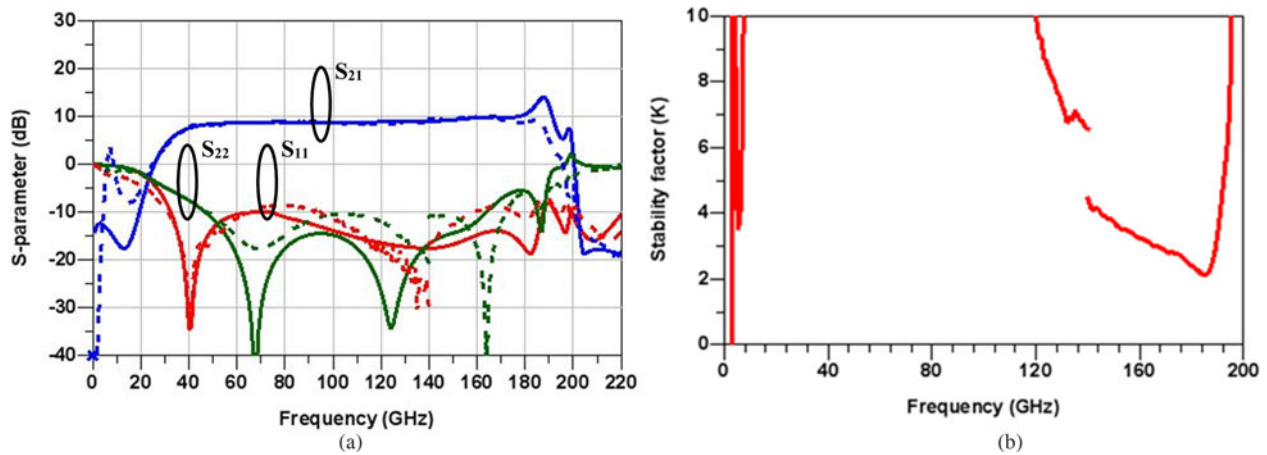


Fig. 10. (a) Simulated (solid line) and measured (dotted line) S-parameters and (b) measured stability factor [15].
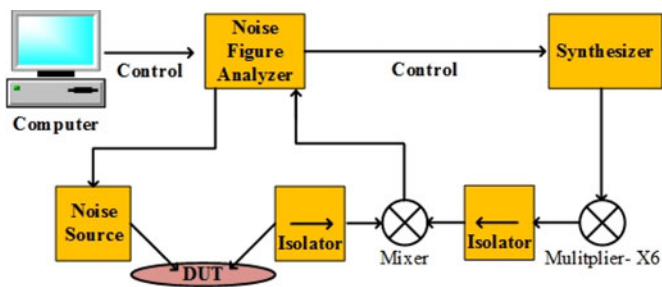


Fig. 11. NF measurement setup.
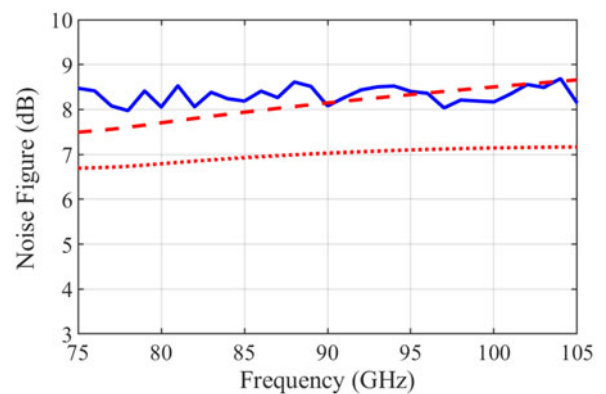


Fig. 12. Measured (solid line) and simulated $NF_{50}$ of the LNA. Dashed line: simulation with noise model assuming $\tau_n = 0$, dotted line: simulation assuming $\tau_n = \tau_{bc}$.

of this ultra-wideband LNDA was therefore based on an extrapolation of a model carefully determined up to only 26 GHz. The good prediction of the LNDAs noise performance prove the validity of the model assumptions up to 100 GHz and beyond, which provides an important contribution to the noise modeling of InP HBTs.

The NF measurements for the frequency range from 75 to 105 GHz are plotted in Fig. 12. The NF is fairly constant with an average value of 8 dB and a variation of ±0.3 dB within this frequency range. This result indicates the circuit's potential for low-noise performance over a very high bandwidth. Even though InP

**Table 1.** State-of-the-art of ultra-broadband LNDA with reports of low noise (gain > 7 dB).

| Ref. | BW (GHz) | Gain (dB) | Technology | Circuit topology | GBP (GHz) | $P_{DC}$ (mW) | $P_{SAT}$ (dBm) | Noise figure (dB) |
|------|----------|-----------|------------|------------------|-----------|---------------|-----------------|-------------------|
| [14] | 235 | 16 | 250 nm InP DHBT | Cascode 2-cascaded[a] | 1483 | 117 | NA | 10 at 100 GHz |
| [11] | 182 | 10 | 250 nm InP DHBT | Cascode 4-cascaded[a] | 575 | 105 | 8.5 at 134 GHz | NA |
| [27] | 180 | 18.7 | 130 nm SiGe HBT | Cascode 3-cascaded[a] | 1550 | 86 | 2.5 at 100 GHz | 6 at 60 GHz |
| [9] | 170 | 10 | 130 nm SiGe HBT | Tricode | 537 | 108 | 9 at 50 GHz | 6.5 at 52 GHz |
| [28] | 160 | 19 | 130 nm SiGe HBT | Tricode | 1426 | 560 | 13.5 at 135 GHz | NA |
| **This work** | **145** | **10** | **500 nm InP DHBT** | **Cascode** | **458** | **96** | **10 at 160 GHz** | **8 at 75–105 GHz** |
| [26] | 135 | 8.5 | 55 nm SiGe BiCMOS HBT-FET | Cascode | 360 | 99 | 10 at 20 GHz | 7 at 90 GHz |
| [30] | 120 | 7.3 | 40 nm GaN DHFET | Cascode | 278 | 448 | 19 at 20 GHz | 6.5 at 20 GHz |
| [25] | 110 | 11 | 50 nm InGaAs mHEMT | Cascode | 390 | 450 | 11 at 75 GHz | 8 at 105 GHz |
| [10] | 96 | 13.5 | 35 nm mHEMT | Cascode | 454 | NA | 15 at 98 GHz | NA |
| [12] | 87 | 7.8 | 120 nm SOI CMOS | Cascode | 137 | 130 | 11 at 20 GHz | 6 at 14 GHz |

[a]Multi stage distributed amplifier.

DHBT-based circuits exhibit inferior noise performance as compared with HEMT devices, the results presented here highlight the potential of InP DHBT for ultra-wideband low-noise applications above 100 GHz.

As discussed above, noise performance was optimized using a noise model neglecting the noise correlation time constant $\tau_n$, depicted by the dashed line in Fig. 12. This curve shows excellent agreement within the estimated range of measurement uncertainty. As a comparison, a post-fabrication simulation was performed assuming $\tau_n = \tau_{bc}$, see dotted line in Fig. 12. This predicted NF is lower, as expected from the investigation of the noise model. The difference in NF obtained with the two model assumptions, however, is less than suggested from the difference in predicted $NF_{50}$ of the device, which is about 3 dB at 105 GHz as seen in Fig. 5. This is caused by the fact that the assumption made for $\tau_n$ affects all four noise parameters including optimum noise match.

With reference to Fig. 10, the measured and simulated gain, $S_{21}$, and input match, $S_{11}$, agree very well. The graph also proves the good quality of the model in terms of predicting the LNDA behavior, but also verifies that the input matching assumed in circuit design was actually realized in the fabrication of the chip. Overall, the LNDA results prove that the modeling assumption based on noise-parameter measurement up to 26 GHz are valid and provide excellent prediction of the noise behavior up to 105 GHz. It is safe to conclude that the proposed noise model will remain valid up to the maximum frequency for which the underlying small- or large-signal model predicts the behavior with good accuracy. As stated before, even though the HBTs minimum NF is increasing with frequency due to the low-noise correlation time constant $\tau_n$, the results obtained with this circuit prove that they are competitive devices for LNDA design.

Table 1 benchmarks the state-of-the-art ultra-wideband LNDAs, arranged in the order of decreasing bandwidth. We note that our circuit has outstanding attributes when compared with the state-of-the-art regarding several metrics: first, it has very high 3-dB bandwidth reported for a single-stage cascode based DA. Second, this circuit exhibits one of the lowest W-band NF values among ultra-wideband LNDA, while going up in frequency to the D-band. Moreover, it has very low DC

power consumption in this class of circuits. In terms of NF, the circuit achieves a value of 8 dB which is fairly constant in the 75–105 GHz range. From the literature, it is seen that the NF increases with increasing frequency beyond 60 GHz [9, 14, 25–27]. Therefore, an NF value of 8 dB is close to the lowest reported NF in W-band for such ultra-wideband LNDAs. Among the circuits in Table 1, only [26] presents a lower NF in W-band than our work, however, it covers DC-135 GHz and thus a lower frequency range than our work, which includes the full D-band. Regarding bandwidth, [9, 14, 27, 28] yield higher bandwidth but the NF values are either worse or not provided in the W-band. In terms of RF power, the maximum RF output power, $P_{sat}$, of 10 dBm at 160 GHz makes the circuit a potential candidate for ultra-broadband, low-noise high-power applications covering W-band and D-band simultaneously. Reports of high and uniform output power of DA using the same technology has been published for lower frequency range [29].

## Conclusions

In this paper, the design of an ultra-broadband LNDA with a low noise is analyzed, which exhibits a high output power $P_{sat}$ of 10 dBm at 160 GHz as well as good low-noise performance, a circuit NF of 8 dB in the 75–105 GHz range and a very low DC power consumption. This work has two-fold novel information regarding the design of ultra-broadband LNDAs. One aspect is the design of the circuit itself which covers both W-band and D-band with high-power characteristics and low-NFs in the W-band. The other aspect is the verification of the noise model which can reliably predict the NF beyond the scope of measurement facility.

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