DOI: 10.1017/S1431927605510043
Microsc Microanal 11(Suppl 2), 2005

Sub-50nm Metrology Control in the Fabrication Processing of Quartz-based Nanoimprint Templates by Variable Pressure SEM Imaging

Dominique Drouin, Eric Lavallée, Mélanie Cloutier, Lau Kien Mun, Jacques Beauvais and Brendan Griffin[1]

Quantiscript Inc., 2500 boul. Universite, Sherbrooke, Québec, J1K 2R1, Canada.
[1]Centre for Microscopy and Microanalysis, the University of Western Australia, Australia.

Manufacturing of microelectronic products requires the constant improvement of fabrication processes. The "International Semiconductor Technology Roadmap" is a 15 years forecast of all the critical characteristics required for microelectronic process fabrication. One critical point within such process is the lithography step that directly drives the performance of fabricated devices. Nowadays, state of the art chips requires 90 to 65 nm critical dimension at the wafer's step. Such features are obtained using short wavelength (193 nm) optical source lithography and post lithography processing. This technique is based on 4x reduction of previously patterned chrome on quartz masks. Sub-optical source wavelength features can be achieved using several corrections at the mask level. The sizes of those corrections are typically at one quarter of the wavelength, which means electron beam tools used to fabricate optical masks require resolutions similar to the size of the wafer printed features. Further reduction of the optical source is technically and financially prohibitive. A few potential candidates are thus investigated as alternate techniques to this 193 nm lithography. Among those, nanoimprint lithography is being pursued by several manufacturers. This technique takes advantage of the direct replication of mask features by mechanically imprinting the topography of the mask within wafer resist, followed in some cases by a UV flash step to cure the resist. This technique requires masks or templates with quartz etched (typically ~100nm depth) and feature critical dimensions equal to the technology node (65nm and below).

To meet ITRS roadmap goals, resists and associated processes for e-beam lithography in the low energy (<3KeV) regime were developped. A vacuum deposited organic resist was used for template fabrication. This presentation will highlight the challenges of controlling features dimensions and line edge roughness (LER) throughout the fabrication steps required for producing a commercial template. The process is composed of several critical steps, such as electron beam resist patterning, transfer of resist patterns in a chrome hard mask and final quartz etch. Following each critical steps, metrology is required to understand their respective contributions to LER and CD variation. Such complete characterization is required in order to apply suitable corrections such as CD bias at pattern level or process improvement to meet final LER target.

Optical inspection of mask features within sub-50nm range is no longer possible. Atomic force microscopy (AFM) or scanning electron microscopy (SEM) techniques are thus required. AFM has not been widely used for templates inspection due to tip artifacts within dense features such as 50nm lines and spaces. SEM inspection at the resist level is routinely used and produces adequate results (Figure 1). The chrome hard mask layer below the resist also acts, in this case, as a charge dissipation layer. After a dry etch transfer of resist pattern in chrome, inspection is not possible as charging effects distort the pattern and change the CD and LER values (Figure 2). At the final step, the chrome patterns are transferred in quartz followed by chrome strip. Direct inspection is again not possible due to charging effects thus a conductive layer is required for SEM investigation. Figure 3 shows 50 nm lines and spaces template coated with a Au/Pd conductive layer. CD and LER can be extracted from such pictures, but the coating layer (Au/Pd) will influence the collected data.

Conductive layer grain size and thickness will directly affect the measured LER and CD values respectively.

The objectives of the presented work are to investigate a low vacuum SEM technique to address the issue of templates metrology within the sub-50 nm range and to assess tool improvements which will be needed to meet roadmap requirements.

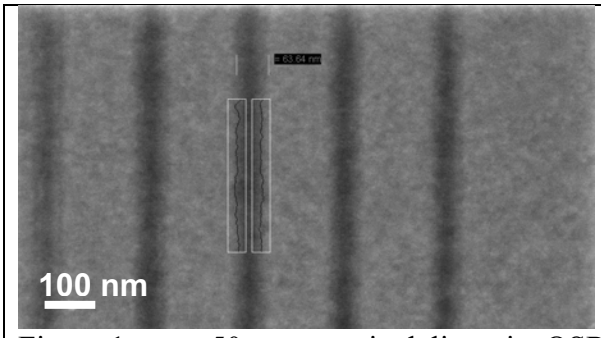

Figure 1 50 nm nominal lines in QSR-5™ resist with 150 nm pitch on chrome layer. Actual sizes are 47.5nm linewidth and 5.4nm 3σ LER.

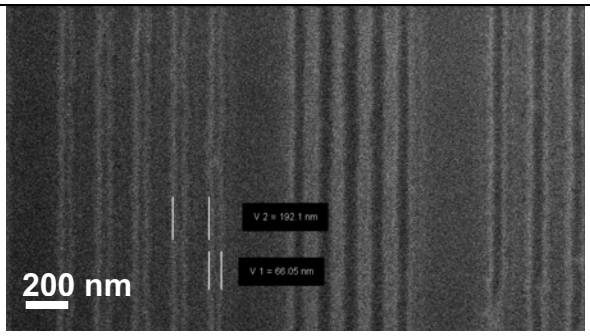

Figure 2 50 nm nominal Cr lines on quartz with 150 nm pitch. Charging effects are preventing accurate measurements of CD and LER.

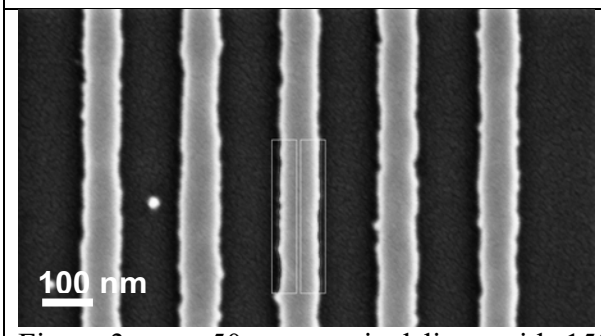

Figure 3 50 nm nominal lines with 150 nm pitch transferred in quartz. A ~10 nm conductive AuPd layer has been deposited to allow observation of the features. Actual size are 79 nm linewidth and 3nm 3σ LER.

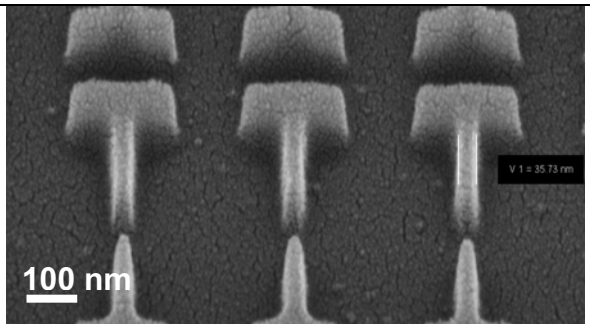

Figure 4 50 nm nominal gate feature on final template. A ~10 nm conductive AuPd layer has been deposited to allow observation.

References:

ITRS, International Technology Roadmap for Semiconductors, (Semiconductor Industry Association), 2004 update, www.public.itrs.net

Spectel Research Corporation, www.spectelresearch.com/measure.html

M.T. Postek and A.E. Vladar, Scanning, vol 26p 11-17 2004.

https://doi.org/10.1017/S1431927605510043 Published online by Cambridge University Press