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Sample Preparation Challenges in Advanced Semiconductor Test Structures

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As semiconductor device structures have continued to reduce in size following Moore's Law and new structures have evolved to address performance needs, transmission electron microscopy (TEM) sample preparation requirements have also needed to adapt and evolve. A number of years ago (~2012) as semiconductor device architecture moved below the 22nm technology node, projection effects due to focused ion beam (FIB) prepared TEM sample thicknesses being larger than single device features became an issue with image interpretation. State-of-the-art FIB sample preparation at the time could routinely produce TEM samples with thicknesses on the order of 50-100nm. For the case study described by Demarest et al. in [1] the test structure examined had a pitch of 200nm. One aspect of the structure was about 160nm wide while the area between was around 40nm wide. The authors of [1] overcame the dimensional challenge by applying a broad beam Argon (Ar) ion mill to further thin the sample post FIB manufacture to less than 30nm in combination with a slight sample rotation (5-10°)with respect to the manufactured structure. This technique did require a doubling of sample preparation time to produce a viable sample. Today's geometrically comparable state-of-the-art semiconductor technology has pitches around 45nm with areas of interest within the structure of about 20nm wide. This sample preparation methodology was used to address projection effect issues for the stacked nanosheet gate all around transistor architecture reported in [2] with a L_g=12nm and 44/48nm contact poly pitch (CPP). Significant care was required to produce samples for this geometry quadrupling the time of a "standard" FIB only prepared sample. As a result the technique was used only when absolutely needed. It did make for outstanding microscopy results as shown in Figure 1 and the technique of [1] was a viable sample preparation method for most of a decade. While the original solution of [1] can still be applied, FIB technology has advanced to the point where it can now repeatedly produce TEM lamella of 20nm thicknesses or less in significantly less time (about 30 minutes) than reported historically in the literature [3]. Figure 2 shows TEM cross sections of a DBFIB TEM cross sectional sample with a thickness on the order of 10-30nms. This process is currently under refinement to target a uniform sample thickness of 20nm with the intent of completely replacing the preparation technique described in [1].

Additional TEM sample preparation challenges can also be presented by novel materials which have sensitivity to certain imaging techniques. For the last several generations of commercial semiconductor devices the low k dielectric materials (e.g. SiCOH), used to insulate the metal wiring on the chips, have shown to contract under electron beam irradiation over the range of 1-30keV from their as manufactured state. In order to develop robust processes for making TEM samples on wafers that have these films and have top down features that are not visible under ion beam imaging, yet are visible under electron beam and optical imaging several approaches have been utilized. One strategy is to use the optical microscope (FOV ~1mm) to get an approximate location of the region of interest (ROI). Ion beam milling removed from the ROI using the ion beam to expose a known feature is performed next (Figure 3). From this known feature a stage move to the ROI is used. From here local deprocessing can take place which allows final targeting of the feature of interest. An alternative technique can be to use the electron beam to locate top down features away from ROI and then creating an electron beam deposition to act as a

fiducial mark (Figure 3). The ion beam can then be used for subsequent targeting with reference to the know fiducial feature.

References:

[1] J. Demarest *et al*, Proceedings from the 37th International Symposium for Testing and Failure Analysis (2013) p. 544.
[2] N. Loubet et al, 2017 Symposium on VLSI Technology (2017) p. T230.
[3] J. Demarest and Z. DeSouza, Proceedings from the 33rd International Symposium for Testing and Failure Analysis (2009) p. 334.

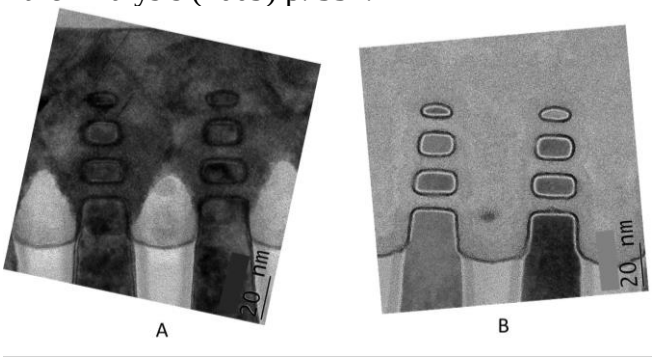

Figure 1. Stacked nanosheet structure reported in [2] with sample preparation technique of [1] applied. As FIB prepared (A) with a sample thickness of about 100nm and after additional thinning (B) with a sample thickness of about 20nm.

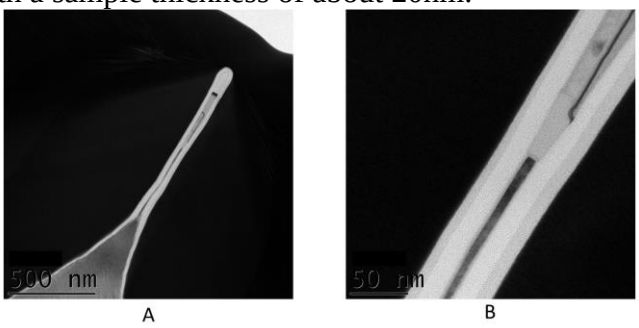

Figure 2. A TEM image of a lamella in cross-section showing the region of interest to be between 10 and 30nm thick. Low magnification (A) and high magnification (B).

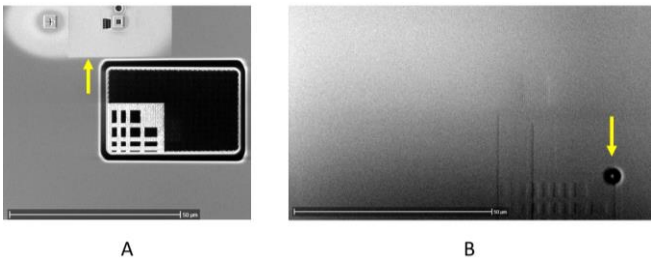

Figure 3. Ion beam exposed feature (A) with subsequent deprocessing and fiducial depositions indicated by the arrow and electron beam deposited fiducial feature as the small circular shape in the lower right indicated by the arrow (B).

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