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Analytical TEM Characterization of Source/Drain Contacts in Advanced Semiconductor Devices

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As the semicondutor industry moves beyond 10 nm to the 7 nm and 5 nm nodes, fundamental innovations are needed to address the scaling challenges. New device architectures, such as Fin Field-Effect-Transistors (FinFETs) and nanosheet/nanowire FETs, have been introduced into industry manufacturing or are currently in research and development phases. Novel materials are also being developed and applied in both front end of line (FEOL) and back end of line (BEOL) device integrations to improve device performances. At the 10 nm node, significant differences are already seen in the middle of line (MOL) architecture and materials used by leading semiconductor companies. This is expected to continue to smaller nodes. Among concerns driving theses industry changes, the impact from rising parasitic resistance and capacitance becomes the bottle neck for improving transistor performance. TEM characterization challenges are increased by the continuous scaling, device transition from 2D to 3D and new materials introduction. In this paper, analytical TEM characterizations on MOL contacts in advanced semiconductor devices will be discussed.

Figure 1(a) shows the cross-sectional view of the conventional trench silicide contact. Figure 1(b) shows a cross-sectional TEM image of a test structure with filled metals (copper and tungsten). The Ti/TiN liner is deposited before W fill. Figure 1(c) shows the high resolution HAADF image of the silicide contact region. There are some drawbacks for the conventional silicide formation process, such as undesired plasma damage to the bottom surface and polymer residue formed during dieletric etch process. In addition, the overetch and post etch cleaning process will gouge the source/drain region. All of these effects will impact the final silicide contact resistance. In order to address these issues, a new integration scheme (epitaxial growth through contact trench) has been developed [1-2]. Figure 2(a) shows the cross-sectional view of the trench epitaxy. Figure 2(b) is the cross-sectional STEM image of the FinFET device built up to the M1 level. EDX elemental analysis in Fig.2 (c) shows the as-grown high Ge atomic% epitaxy on top of the source/drain SiGe epitaxial layer. Quantitative EELS analysis (Fig.2 (d)) indicates the trench epi is close to 100% (pure) Ge.

Due to the complex geometry of FinFET devices and the small dimensions of different structures (less than the thickness of the TEM specimen), it is not possible to avoid the projection effects during TEM analysis. In addition, preparation of such specimens at the exact location of interest is difficult and one loses the 3D overview of the whole strucuture in thin specimens. In order to overcome these problems, EDX tomography is used to reveal the structural details in 3D dimensions. Figure 3(a) shows the EDX tomograpy of the trench silicide test structure. Figure 3(c) and (d) show the orthoslice view extracted from the reconstructed EDX tomography data set with and without Cu via. The void/seam in the filled tungsten can be clearly seen. This technique can also be used to evaluate the conformality of the Ti/TiN liner which is useful in determining the surface area of the contact metal to the epi surface, especically on a surface with non-planar topography.

With continuous dimensional scaling, the volume of conducting material (e.g., tungsten) in the metal contact region shrinks, resulting in increasing resistance. One promising option for this fill material in advanced technology node is to use a new material (e.g., cobalt) to replace W[3-6]. Figure 4 shows a

FinFET device using Co as the fill material. The low-angle annular dark field imaging condition is used to reveal more details of the grain strucutres, as shown in Fig.4(b). In addition, the texture or orientation mapping and grain size of the Co contacts will be analyzed by precession electron diffraction (PED) technique since they easily correlate with the eletrcial properties, such as resisitivity.

In summary, comprehensive analytical (S)TEM characterization techniques, including HRSTEM, EDX/EELS spectrum imaging, EDX tomography, precession electron diffraction (PED) are used to study the materials and structures of the middle of line metal contacts in advanced semiconductor devices [7].

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[7] This work was performed by the Research Alliance teams at various IBM Research and Development Facilities.

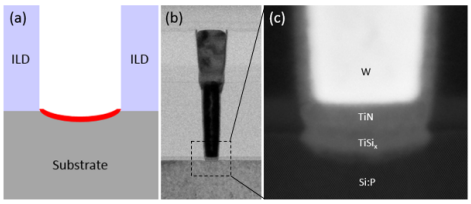

Figure 1. (a) Schematic view of conventional trench silicide; (b) Test structure after metal fill; (c) High resolution HAADF image of the trench silicide.

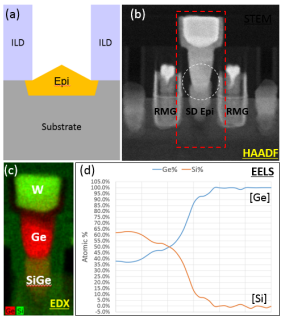

Figure 2. (a) Schematic view of trench epitaxy contact; (b) Dark field STEM image of the FinFET device built up to M1 level; (c) EDX elemental mapping from the contact region; (d) Relative quantitative EELS Si and Ge profiles.

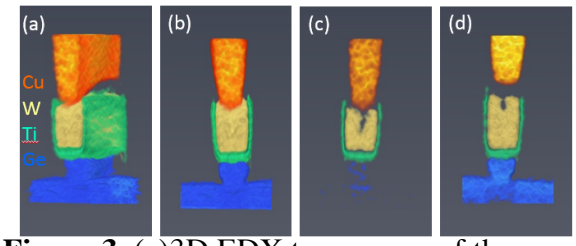

Figure 3. (a)3D EDX tomograpy of the trench silicide test structure; (b) Orthoslice view extracted from the reconstructed entire 3D EDX tomogrpahy data set; (c) Orthoslice view extracted from Cu via; (d) Orthoslice view extracted from the location without Cu via.

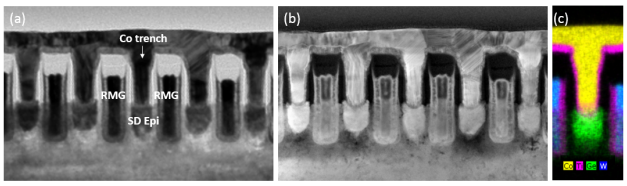

Figure 4. (a) Cross-sectional TEM of the FinFET device using Co contact; (b) low-angle annular dark field image to reveal more details of the grain strucutres; (c) EDX elemental map of the Co contact on top source/drain epitaxy.

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