International Journal of Microwave and Wireless Technologies

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Multilayer substrate integrated waveguide six-port junctions with embedded resistive films

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Research Paper

Cite this article: Tegowski B, Koelpin A (2024) Multilayer substrate integrated waveguide six-port junctions with embedded resistive films. *International Journal of Microwave and Wireless Technologies*, 1–9. https://doi.org/10.1017/S1759078724000680

Received: 9 February 2024
Revised: 11 June 2024
Accepted: 13 June 2024

Keywords:
interferometer; K-band; six-port; substrate integrated waveguide (SIW); thick-film resistor

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Abstract

This article deals with multilayer substrate integrated waveguide (SIW) six-port junctions with embedded carbon resistive films. SIW six-ports usually employ reactive power dividers, which degrade the amplitude and phase balance when the six-port is terminated with mismatched power detectors. The associated impairments are studied and two SIW six-port junctions with improved isolation and output matching are designed for K-/Ka-band applications to overcome these limitations. The proposed designs differ with respect to the configuration of the output ports making the underlying six-port topology applicable for different layout requirements. Measurements of the fabricated components validate the concept. The six-ports are compact, fully shielded and can be integrated in multilayer printed circuit boards.

Introduction

High-precision remote distance sensing using radar [1], direction-of-arrival detection [2], and communication receiver systems [3] are just a few examples of numerous microwave and millimeter-wave applications whose working principles rely on phase difference measurements. Besides mixer-based approaches, these can be conducted with six-port interferometers, which are low-cost, easy to implement, and provide high resolution [1]. Here, the phase difference of two input signals is determined from the powers of four output signals obtained by superimposing the inputs under four different relative phase shifts.

Six-port junctions have been realized in different technologies such as microstrip [3], waveguide [4], and substrate integrated waveguide (SIW) [5–8] using quadrature hybrid couplers, power dividers and phase shifters. Waveguides outperform components implemented on printed circuit boards (PCB), such as microstrip and SIW, regarding material losses, but they are heavy and costly. Microstrip technology is advantageous as it supports surface-mounted devices (SMD) for matched terminations or Wilkinson power dividers. However, it is inferior to SIW and waveguide technology with respect to shielding. SIWs implement waveguide-like properties on PCBs [9, 10] and have been subject of extensive research over the last 20 years, which yielded a multitude of passive component implementations including their miniaturization and transitions to different transmission line types.

SIW six-ports usually employ *H*-plane components with reactive power dividers [5–7], which, in addition to large size, results in poor matching and isolation of their output ports. As a consequence, mismatched outputs, e.g., caused by diode power detectors, distort the amplitude and phase relationships under which the input signals are superimposed. Although *H*-plane SIW power dividers with sufficient isolation are realizable, they either require the insertion of slots bridged by SMD resistors [11], or terminations of additional ports [12], which impairs shielding and compactness, respectively. In contrast, *E*-plane SIW dividers are based on a bifurcation, in which a thick-film resistor can be deposited, which enhances output matching and isolation [13, 14].

Tegowski and Koelpin [8] introduce a multilayer SIW six-port approach by combining *E*-plane power dividers with *H*-plane couplers. This concept achieves a small footprint and additionally provides an alternative layout of in- and output ports compared to conventional SIW six-ports [5–7]. As illustrated by the generic schematic in Fig. 1(a), the inputs and the output pairs are orientated anti-parallel and, thus, located on opposing sides in a conventional six-port. In the stacked six-port concept, see Fig. 1(b), the inputs run parallel next to each other and all outputs are located on the side opposing the inputs. This configuration inherently separates radio-frequency from baseband circuitry, which is connected to the outputs.

Although the stacked concept achieves a small footprint compared to other SIW six-ports [8], it likewise suffers from being prone to mismatched outputs because of the applied reactive dividers. By enhancing the output matching and isolation through embedded

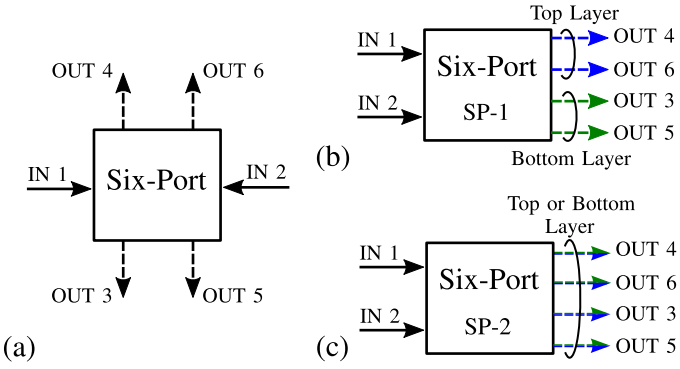

Figure 1. Port configuration of (a) a conventional six-port, (b) the multilayer stacked SIW six-port concept from [8, 15], and (c) its proposed extension.

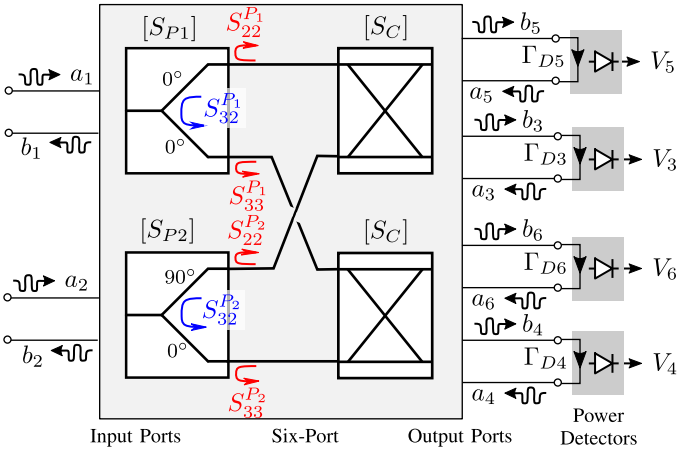

Figure 2. Block diagram of a six-port junction terminated with power detectors.

carbon resistive films, [15] advances the above six-port concept regarding its electrical performance. The improvement maintains the small footprint of [8], thus, yielding a compact and robust SIW six-port. However, the output ports in the stacked SIW topology presented in [8] and [15] are located on both sides of a symmetrical three-layer PCB, see Fig. 1(b). Depending on system and PCB layout requirements, for instance, resulting from separation of antennas and RF circuitry [2] this output port configuration may be unfavorable.

This article extends the work presented at the 2023 53rd European Microwave Conference and published in its proceedings [15] by proposing a modified stacked SIW six-port design. It is equipped with tailored transitions, which transfer all outputs either to the top or the bottom layer, see Fig. 1(c). The amplitude balance is corrected using an asymmetric layer stack.

Section "Fundamentals" reviews six-port fundamentals with emphasis on output matching and isolation. Section "Six-Port Design" describes the design of stacked SIW six-port junctions with integrated resistive films. Besides, it outlines the augmentation approach. Section "Manufacturing and Measurement Results" presents the fabrication and the experimental validation. Section "Conclusion" concludes the article.

Fundamentals

Figure 2 depicts the block diagram of a six-port junction terminated with diode power detectors. Here, the six-port consists of two quadrature hybrid couplers, one inphase and one quadrature power divider. These components superimpose the two input signals a_1 and a_2 under four different relative phase shifts (0°, 90°, 180°, 270°). The detectors convert the power of the output waves b_i ($3 \leq i \leq 6$) to voltages, which, assuming ideal square-law characteristic, obey the relative phase difference $\varphi_{12} = \arg(a_1/a_2)$ between the input signals follows from [1]:

$$V_i \propto |b_i|^2 \cdot (1 - |\Gamma_{Di}|^2). \tag{1}$$

$$\varphi_{12} = \arg\{ \underbrace{(V_5 - V_3)}_{=I\,(\text{Inphase})} + \jmath \underbrace{(V_6 - V_4)}_{=Q\,(\text{Quadrature})} \}. \tag{2}$$

Because of the non-zero reflection coefficient at the detectors Γ_{Di}, the output waves b_i are partially reflected and reenter the six-port. The output port matching and output-to-output isolation then determine the magnitude and phase according to which these secondary signals appear at all six-port outputs and thereby degrade the originally constituted amplitude and phase balance. As illustrated in Fig. 2, reactive power dividers mainly contribute to this degradation. Being a reactive three-port network, they cannot simultaneously be matched and isolated at all their ports [16], and thus, establish multiple closed loops within the six-port. In particular, for perfect input matching and equal power split, their output return loss and isolation is only 6 dB. Accordingly, the six-port itself shows poor output matching and isolation between its output ports. Figure 3(a) studies the above effect for $\Gamma_{Di} = \Gamma_D$ ($3 \leq i \leq 6$) in the IQ-diagram. It is synthesized according to (1), (2), and the schematic from Fig. 2, which is excited by two input signals with unity magnitudes and varying phase difference. The couplers are assumed to be ideal in terms of return loss and isolation. For a six-port with ideally matched and isolated power dividers ($S_{ii}^{P_j} = S_{32}^{P_j} = 0$), increasing Γ_D leads to a diminished radius as less power is delivered to the detectors. In contrast, a six-port

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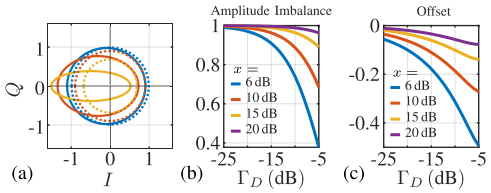

Figure 3. (a) *IQ*-diagram of a six-port with reactive (solid) and ideal (dotted) power dividers for different output reflection coefficients $\Gamma_D = -20$ dB (blue line), $\Gamma_D = -10$ dB (red line), and $\Gamma_D = -5$ dB (yellow line). (b) Amplitude imbalance and (c) inphase offset versus Γ_D for a six-port with power dividers exhibiting an output return loss and isolation of x.

with reactive dividers ($|S_{ii}^{P_j}| = |S_{32}^{P_j}| = 0.5$) suffers from significant deformation of the circle to an ellipse, which is offset with respect to the origin. Fig. 3(b) and (c) reports the amplitude imbalance and offset of the *IQ*-characteristics [1]. Power dividers with output return loss and isolation better than 20 dB make the six-port quite robust even for large mismatches. Otherwise, an individual calibration unique for a particular Γ_D becomes inevitable. To improve the six-port robustness in this respect, dividers with resistive elements must be applied.

Six-port design

The herein considered K-/Ka-band SIW six-port design, shown in Fig. 4, accords with the block diagram from Fig. 2 and relies on the concept introduced in [8]. It stacks two cruciform H-plane quadrature hybrid couplers using a three-layer stack (heights h_{12} and h_{23}) and employs one inphase and one quadrature E-plane power divider. The latter is based on the concatenation of a bifurcation with a phase shifter, which is realized by the combination of stacked unequal-width equal-length and delay-line phasers integrated in three 90°-bends [8, 17]. The output port pairs P3-P4 and P5-P6 are each positioned on top of each other, which yields the topology indicated in Fig. 1(b). To improve the output matching and isolation of the six-port, carbon resistive films are introduced as illustrated in Fig. 4. This preserves the advantages of

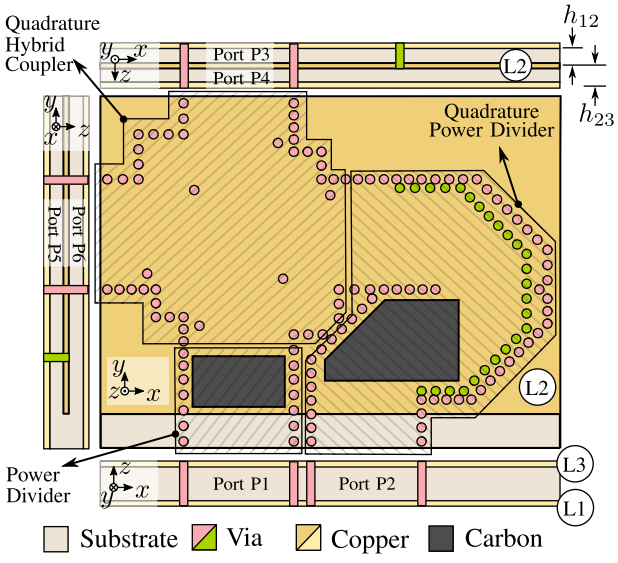

Figure 4. Schematic of the six-port junction SP-1. Layers L1 and L3 consist of plain copper.

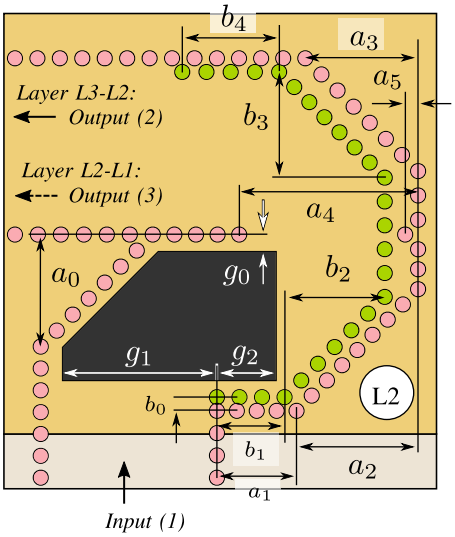

Figure 5. Schematic of the quadrature power divider with embedded resistive film. Port 1 denotes the input port, port 2 is the upper (layers L3–L2) and port 3 the lower (layers L2–L1) output. Dimensions in mm: $\{a_0\ a_1\ a_2\ a_3\ a_4\ a_5\} = \{3.04, 2.16, 3.3, 3.06, 4.86, 0.35\}$, $\{b_0\ b_1\ b_2\ b_3\ b_4\} = \{0.37, 1.84, 2.72, 2.87, 2.63\}$, $\{g_0\ g_1\ g_2\} = \{1.1, 4.19, 1.61\}$.

compactness and integrability in multilayer PCBs while improving the output port matching and the output-to-output isolation. Design details of the quadrature hybrids and the E-plane power divider with a resistive layer can be found in [18, 19] and [13, 14], respectively. Using a power divider with a resistive film (similar as at port P1) in front of the phase shifter, would enlarge the footprint, which is unfavorable. Thus, the resistive film is here integrated in the phase shifting section. The six-port is designed by individually optimizing its subcomponents using *CST Microwave Studio*. The substrate used is *Megtron 6* with a relative permittivity of $\epsilon_r = 3.62$ and loss tangent $\tan\delta = 0.005$. The nominal SIW width $a_{\mathrm{SIW}} = 4.78$ mm corresponds to a cutoff frequency of 17.4 GHz. First, a symmetric layer stack with $h_{12} = h_{23}$ is considered such as to achieve an equal power split by the E-plane dividers. Note that the behavior of the subcomponents is invariant with respect to the substrate height due to the fundamental TE_{10}-mode operation. This six-port junction is referred to as SP-1 in the following.

Quadrature power divider with integrated resistive films

The quadrature power divider, whose schematic is provided in Fig. 5, is designed in three steps. The respective intermediate results are presented in Fig. 6. Figure 6(a) depicts the isolation, the in- and the output matching, Fig. 6(b) the amplitude ratio, and Fig. 6(c) the phase balance.

First, the resistive layer is disregarded and the parameters a_i and b_i are optimized with respect to input matching, amplitude balance, and quadrature phase shift [8]. A $\pm 2°$-phase shift flatness between 22 and 28 GHz is targeted. The optimization results are presented in dotted lines in Fig. 6. Since the divider is reactive, the output matching and isolation are only about 7 dB including material losses. In the next step, the resistive region is inserted in layer L2. Amplitude and phase imbalances of the fields in the upper (between L3 and L2) and lower SIW (between L2 and L1) lead to a current in the resistive film, which dissipates the associated power. This establishes matching and isolation of the output ports

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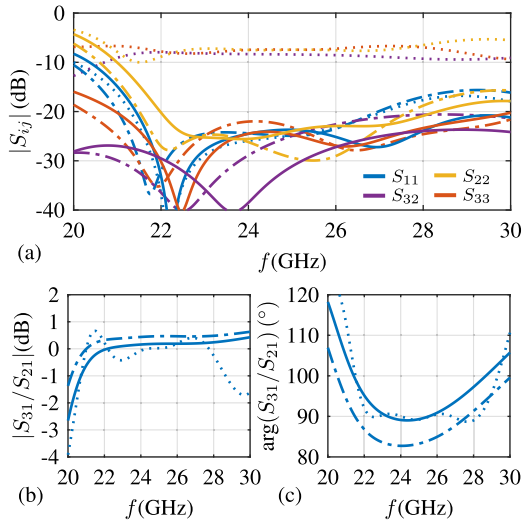

Figure 6. Simulation results of the quadrature power divider after three optimization steps: without resistive film (dotted), with inserted resistive film (dash-dotted), after final re-optimization (solid).

depending on the conductivity σ_c, thickness t_c and length of the resistive film [14]. Based on a preliminary experimental study, the conductivity of the employed resistive material is determined as $\sigma_c = 2200\,\mathrm{S/m}$. Besides, a thickness of $t_c = 10\,\mu\mathrm{m}$ is considered. The unequal widths of the upper and lower SIW gradually increase the phase shift between the divided parts of the input signal, thus, generating a current density, which increases toward the end of the phase shifter. As this would impair the insertion loss, the resistive layer is located at the beginning of the phase shifting section, where the phase imbalance is small. The resistive layer length is optimized to achieve an output matching and isolation better than 20 dB. The resulting performance is represented by dash-dotted lines in Fig. 6. The resistive film significantly improves the isolation and output matching compared to the first design step.

Since the resistive layer modifies the SIW propagation constant the initially established phase balance is slightly distorted. This is corrected by a re-optimization of the SIW boundaries, which besides considers all aforementioned goals and minimizes the phase shift error around 24 GHz. As a result, matching and isolation satisfy 20 dB and the phase shift is within $92^\circ \pm 5^\circ$ from 22 to 28 GHz, see solid lines in Fig. 6.

Extended six-port

The stacked configuration of the output ports P3–P4 and P5–P6 requires to locate power detectors on both sides of the PCB making the stacked six-port concept SP-1 inconvenient for applications which do not support double-sided component placement. To resolve this drawback, six-port SP-1 can be implemented on an asymmetric layer stack and extended by appropriate transitions connected to its outputs. Figure 7 illustrates this concept, which will be referred to as six-port SP-2 in the following.

Figure 8 presents the schematic of the proposed output transition. It transfers the two stacked SIWs coming from the six-port outputs, to two SIWs located next to each other on the top layer L3. For this, the lower SIW first reverses its propagation direction by means of two consecutive mittered H-plane 90°-corners. To rout the signal propagating in the lower SIW to the upper layer, it then passes through an E-plane 180°-corner. It is implemented

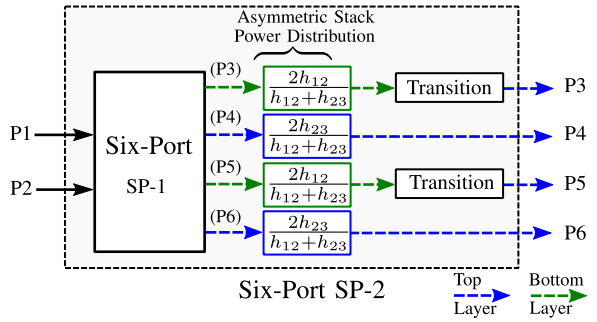

Figure 7. Conceptual block diagram of six-port SP-2 with $h_{12} > h_{23}$.

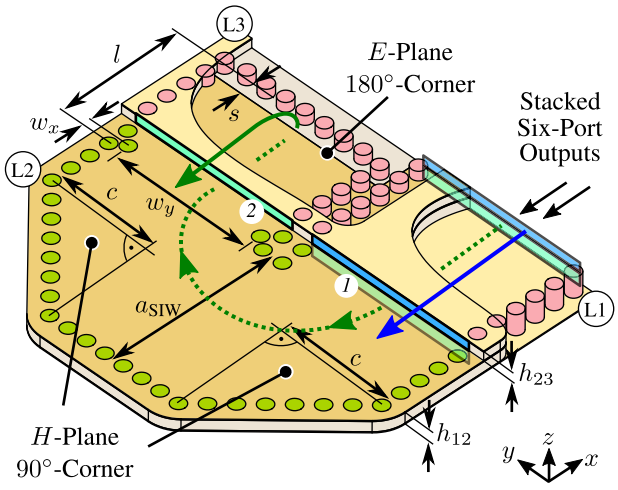

Figure 8. Schematic of the output transition. The cutouts in the substrate serve visualization purposes. Dimensions: $w_x = 0.27\,\mathrm{mm}$, $w_y = 4.08\,\mathrm{mm}$, $l = 3.61\,\mathrm{mm}$, $s = 0.41\,\mathrm{mm}$, $c = 3.10\,\mathrm{mm}$, $h_{12} = 0.3\,\mathrm{mm}$, $h_{23} = 0.25\,\mathrm{mm}$.

by partially removing the middle copper layer L2 and connecting the outer layers with a via row placed at distance s. Parameter c and the iris with opening w_y located at position $l - w_x$ adjust the matching of the transition. The upper SIW is continued unaltered to a common reference yz-plane.

Because the six-port already superimposed the input signals under the four relative phase shifts and the phase difference information of the input signals is obtained from the power of the outputs [see (1) and (2)], the unbalanced phase accumulation due to the transition is inconsequential. However, the additional losses associated with the increased path length of the lower signal, disturb the amplitude balance originally established by the six-port. To compensate for this, the layer stack is implemented asymmetric with $h_{23} < h_{12}$. This is purposeful since the E-plane dividers split the incident power according to the height ratios $h_{23}/(h_{12} + h_{23})$ and $h_{12}/(h_{12} + h_{23})$ for the SIW between layers L2–L3 and L1–L2, respectively. Accordingly, the unequal power split is selected such as to equalize the transition insertion loss of the bottom SIW. In this case, the height ratio h_{12}/h_{23} satisfies

$$\mathrm{IL}_{\mathrm{dB}}^{\mathrm{Trans}} - 10\log_{10}\left(\frac{h_{12}}{h_{23}}\right) - \mathrm{IL}_{\mathrm{dB}}^{\mathrm{c,12}}\left(\frac{h_{12}}{h_{23}} - 1\right) = 0, \qquad (3)$$

where $\mathrm{IL}_{\mathrm{dB}}^{\mathrm{Trans}}$ is the total insertion loss (in dB) of the transition and $\mathrm{IL}_{\mathrm{dB}}^{\mathrm{c,12}}$ is the mean insertion loss (in dB) associated with conductive losses of six-port SP-1 (implemented with height h_{12})

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excluding 6 dB power division loss. Since for fundamental TE_{10}-mode operation dielectric losses do not scale with the SIW height [16], they cancel out in the loss balance (3). $IL_{dB}^{c,12}$ is estimated by full-wave simulation of the forward transmission magnitudes considering the dielectric as lossfree. Setting $h_{12} = 0.3$ mm, one obtains $IL_{dB}^{c,12} = 0.4$ dB and $IL_{dB}^{Trans} = 0.8$ dB, which based on (3) leads to $h_{23} \approx 0.25$ mm. Note that the concept equivalently applies to transfer the outputs to the bottom instead of the top layer.

Figure 9 shows the simulated scattering parameters of the transition, which is optimized for the determined asymmetric layer stack. From 22 to 29 GHz, the matching exceeds 19 dB.

Manufacturing and measurement results

The quadrature power divider and both six-port designs SP-1 and SP-2 are fabricated with standard PCB processing techniques on *Panasonic Megtron 6* substrates with a relative permittivity (loss tangent) of 3.62 (0.005). The layer stacks shown in Fig. 10 implement a symmetric stack for the quadrature power divider and six-port SP-1 (Fig. 10(a)), and an asymmetric stack for six-port SP-2 (Fig. 10(b)), respectively. To manufacture the resistive films, first a cavity is etched in layer L2, which is filled with *Peters SD 2843 HAL* carbon conductive-ink. After curing, the PCB is manually sanded to achieve a flat surface and the desired thickness. Subsequent electroplating completely covers the carbon film with copper, which is then freed during structuring of layer L2 expect for a small surrounding overlap. This ensures proper electrical contact at the edges [20].

Quadrature power divider

Figure 11 presents the manufactured quadrature power divider with indicated calibration reference planes at which a three-port unknown-through-open-short-match (UOSM) calibration with two offset shorts instead of an open and a match standard is performed. The reference planes are accessed via SIW-to-grounded-coplanar-waveguide transitions and coaxial connectors. Figure 12 presents the simulation and the measurement results acquired by a vector network analyzer (*Rohde&Schwarz ZVA50*). The input return loss is better than 19 dB from 21 to 28.5 GHz. The output return losses exceed 13 dB and the isolation 19 dB from 22 to 28 GHz. The discrepancy compared to simulation results is related to manufacturing tolerances including the conductivity variance of the carbon conductive-ink [14]. The amplitude and phase balance deviate by less than 0.5 dB and 5° in measurement, respectively.

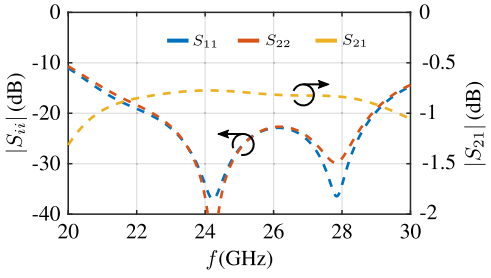

Figure 9. Simulation results of the output transition. Port denomination is indicated in Figure 8.

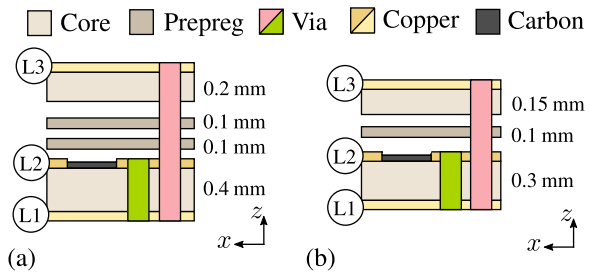

Figure 10. Layer stacks of (a) the quadrature power divider and six-port SP-1, and (b) six-port SP-2.

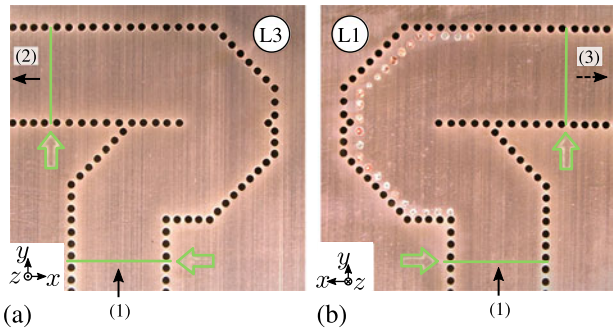

Figure 11. Photograph of the manufactured quadrature power divider.

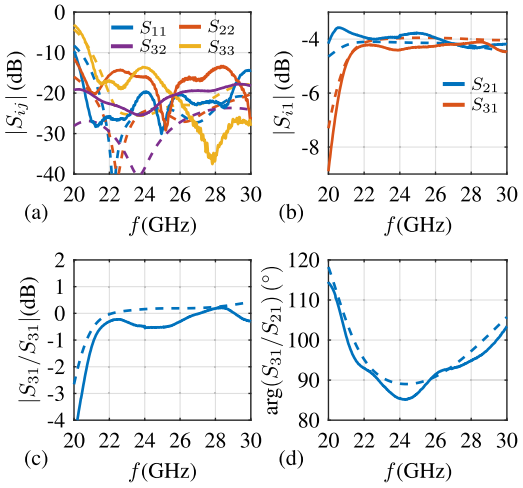

Figure 12. Simulation (dashed) and measurement results (solid) of the quadrature power divider.

Six-port junctions

Figures 13 and 14 present the manufactured six-ports SP-1 and SP-2, respectively. Figure 13(a) and (b) shows an intermediate fabrication result after depositing the carbon film and drilling the vias between layers L2 and L1. The fabricated prototypes are characterized with a four-port vector network analyzer (*Rohde&Schwarz ZVA50*) by measuring ports {P1, P2, P3, P4}, {P1, P2, P5, P6}, and {P3, P4, P5, P6}, respectively. Unused ports are terminated with a matched load. 2.92 mm-connector jacks (*Rosenberger 02K80F-40ML5*) and appropriate transitions are provided to access the SIW ports as shown in Figs, 13(d)–(e) and 14(a), respectively. The calibration planes correspond with the connector reference

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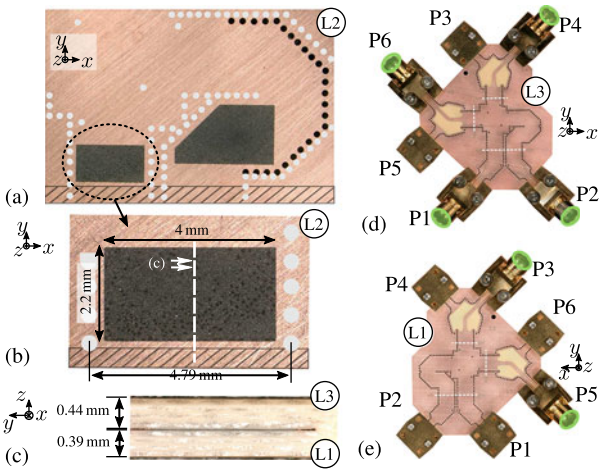

Figure 13. (a) and (b) Photographs of the manufactured six-port SP-1 after deposition of the carbon resistive films. White circles indicate the L1-L3-vias yet to be drilled and hachures mark areas of layer L2 which will be removed. (c) Cross section at the position indicated in Figure 13(b). (d) and (e) Fabricated six-port SP-1 with transitions and coaxial connectors.

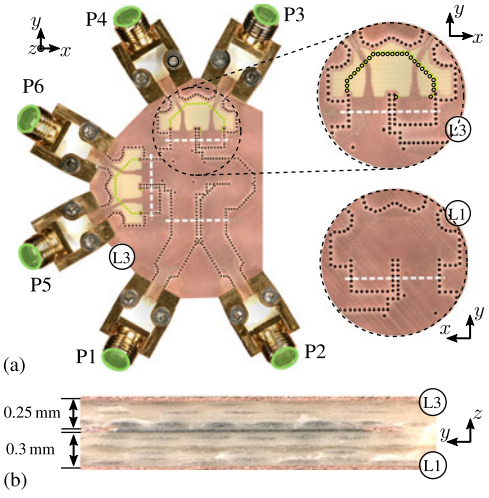

Figure 14. (a) Photographs of the manufactured six-port SP-2 with indicated vias between layers L2 and L3. (b) Layer stack cross section.

planes highlighted in green. For comparability, the simulation results account for the entire transitions including the 2.92 mm-connectors, which in total show a simulated maximum insertion loss of 1.0 dB. Dimensions not reported in this article are consistent with those in [8].

Six-port SP-1

Figure 15(a) presents the input matching and input-to-input isolation of six-port SP-1, which qualitatively agree with the simulation. From 22 to 30 GHz, the matching is better than 17 dB, while the isolation exceeds 20 dB above 22.5 GHz. The forward transmission coefficients responsible for the intended superposition of the input signals are evaluated in Fig. 15(b)–(e). The in-band transmission magnitude varies around $|S_{i1}| = -8.5$ dB and $|S_{i2}| = -9.5$ dB, respectively. This leads to a transmission ratio $|S_{i1}|/|S_{i2}|$ (Fig. 15(d)) of approximately 1 dB, which is related to the additional electrical length of the phase shifter. For both input ports

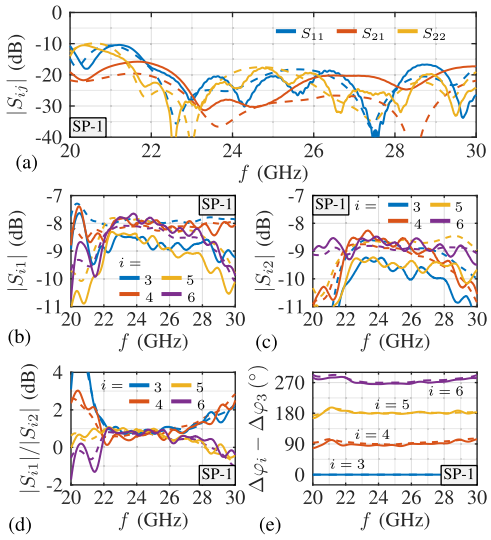

Figure 15. Measurement (solid) and simulation (dashed) results of six-port SP-1. (a) Input reflection coefficients and transmission magnitude S_{21}. (b) and (c) Forward transmission magnitudes and (d) their ratio. (e) Phase differences $\Delta\varphi_i = \arg(S_{i1}/S_{i2})$ relative to $\Delta\varphi_3$.

P1 and P2, the measured transmission to ports P3 and P5 is smaller than the one to ports P4 and P6. This imbalance results from a minor asymmetry of the fabricated layer stack (see Fig. 13(c)) being caused by the two layers of prepreg used to enhance the adhesion during bonding. Thus, in contrast to simulation, an unintended, unequal power split by the *E*-plane bifurcations results. As reported in Fig. 15(e), the fabricated six-port constitutes the required relative phase differences. From 22.5 to 28.5 GHz, the maximum absolute deviation with respect to the intended values is less than 6.5°.

The introduced resistive layers limit the output return loss (Fig. 16(a)) to 13 dB between 22 and 28.5 GHz. Discrepancies between simulation and measurement are associated with thickness and conductivity tolerances of the resistive film [14] as well as its structural inhomogeneity and porosity (see Fig. 13(b)). The latter effect could be mitigated by multiple subsequent carbon deposition and sanding processes. At 24 GHz, a matching better than 19 dB is achieved at all ports. Because of the six-port topology, the output-to-output transmissions can be grouped into three pairs: S_{65} and S_{43} (superposed outputs), S_{63} and S_{54} (crosswise superposed outputs), and S_{53} and S_{64} (outputs of the same couplers). Above 23 GHz, the output-to-output isolation, reported in Fig. 16(b), exceeds 20 dB. As in simulation, the respective pairs exhibit similar progression over frequency. The reduction of isolation for S_{53} and S_{64} toward lower frequencies is dictated by the isolation of the quadrature hybrids. Since the connector transitions only add about 2 dB to the measured insertion loss, the introduced resistive films establish the improvement in output matching and isolation. Meanwhile, the occupied area of six-port SP-1 (as depicted in Fig. 4) is 204 mm^2 and, thus, the same as in [8].

Six-port SP-2

As shown in Fig. 17(a), six-port SP-2 achieves an input matching better than 15 dB above 22 GHz in measurement. The isolation is more than 20 dB in accordance with simulation. The forward transmission magnitudes shown in Fig. 17(b) and (c) vary

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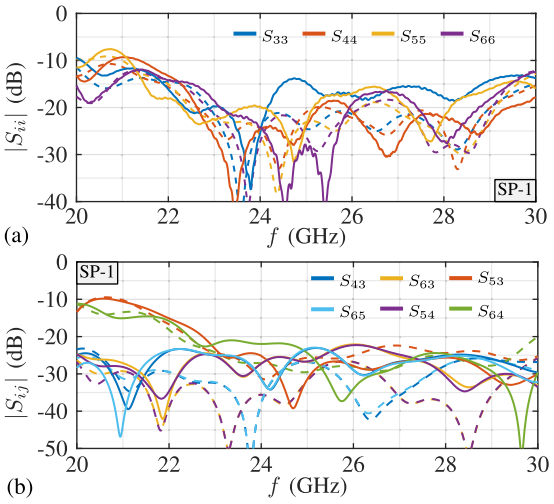

Figure 16. Measured (solid) and simulated (dashed) (a) output reflection coefficients and (b) output-to-output transmission coefficients of six-port SP-1.

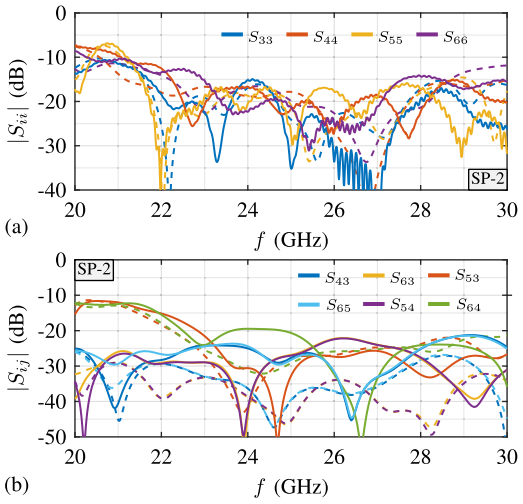

Figure 18. Measured (solid) and simulated (dashed) (a) output reflection coefficients and (b) output-to-output transmission coefficients of six-port SP-2.

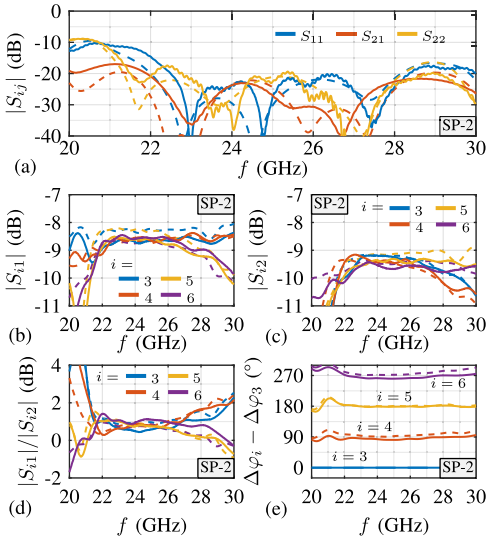

Figure 17. Measurement (solid) and simulation (dashed) results of six-port SP-2. (a) Input reflection coefficients and transmission magnitude S_{21}. (b) and (c) Forward transmission magnitudes and (d) their ratio. (e) Phase differences $\Delta\varphi_i = \arg(S_{i1}/S_{i2})$ relative to $\Delta\varphi_3$.

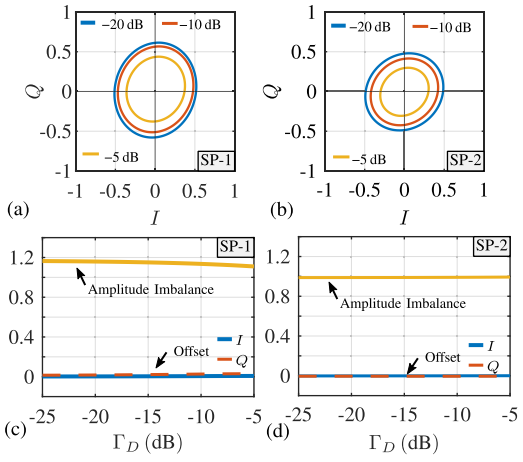

Figure 19. (a) and (b) Synthesized *IQ*-diagrams based on measured scattering parameters of (a) six-port SP-1 and (b) SP-2 for different termination reflection coefficients Γ_D. (c) and (d) Associated amplitude imbalance and *IQ*-offsets for (c) six-port SP-1 and (d) SP-2.

about $|S_{i1}| = -8.7$ dB and $|S_{i2}| = -9.7$ dB, respectively. The combination of the intentionally achieved layer stack asymmetry, see Fig. 14(b), and the output transition losses equalize the transmission magnitudes to all output ports. The increased insertion loss to ports P3 and P5 compared with simulation is linked with increased losses of the output transition, which, however, favors the amplitude balance. The relative phase differences evaluated in Fig. 17(e) deviate by less than 10° from the intended ones within 22 to 28 GHz.

The output return loss, shown in Fig. 18(a), is better than 12 dB above 22 GHz. The output-to-output isolation (Fig. 18(b)) behaves similar as for SP-1. Above 23 GHz, it exceeds 19 dB for all output port combinations.

The output transitions increase the area occupied by SP-2 to 227 mm^2 on the top layer L3 and 348 mm^2 on the bottom layer L1. However, diode power detectors can be placed on layer L3 above the SIW output transition without affecting it.

IQ-diagrams and comparison

To verify the robustness of both six-port designs with respect to output mismatch, Fig. 19(a) and (b) examines synthesized *IQ*-diagrams for different output terminations. These are calculated by solving for the magnitude of the outgoing waves b_3, b_4, b_5, and b_6 (as defined in Fig. 2) if two input waves a_1 and a_2 with equal amplitude but varying relative phase shift are supplied. For this, the measured scattering parameters of SP-1 and SP-2 are employed, respectively. The slightly elliptical shapes stem from the unintended layer stack asymmetry of the manufactured component in case of SP-1 (see Fig. 13(c) and the increased phase imbalance in case of SP-2, respectively. However, an increasing termination reflection coefficient does not distort the *IQ*-characteristic for both designs, which proves the achieved enhancement in output matching and isolation compared to purely reactive SIW six-ports. Fig. 19(c) and (d) support this finding, as the retrieved amplitude

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Table 1. Comparison of SIW six-port junctions

Ref.	f_{c1}	f_{c2}	ISO_{OUT}	RL_{OUT}	RE	ϵ_r	A'_{c1}
[5]	22	30[a]	12[b]	12[b]	yes	2.94	6.16
[6]	22	26[a]	6[b]	9[b]	no	2.2	13.1
[8]	21.5	28.8	6[b]	6[b]	no	3.62	3.77
SP-1	21.8	30[a]	22	17	yes	3.62	3.9
SP-2	22	30[a]	22	18	yes	3.62	4.43[c]

f_{c1}, f_{c2}: lower/upper frequency limit (in GHz) for input return loss larger than 15 dB.
ISO_{OUT}: output-to-output isolation (in dB).
RL_{OUT}: output return loss (in dB).
RE: contains resistive elements.
A'_{c1}: area normalized to squared substrate wavelength at f_{c1}.
[a]: limit by measurement range.
[b]: theoretical values based on block diagram (no measurement results).
[c]: top layer, bottom layer: $A'_{c1} = 6.78$.

balance and offset are fairly flat over the considered range of mismatch values. From $\Gamma_D = -25$ dB to $\Gamma_D = -5$ dB, the change in amplitude balance is below 5%.

Table 1 compares SP-1 and SP-2 with SIW six-port junctions presented in literature, focusing on output matching and isolation performance as well as size. The designs in [5] and [6] rely on a two-layer stack whereas [8], SP-1, and SP-2 require a three-layer stack. The design in [5] implements the six-port with an input quadrature hybrid instead of a quadrature power divider. The additional residual port is terminated by a thin titanium film deposited on the top layer, which enhances output return loss and isolation compared to the entirely reactive designs in [6] and [8]. The proposed six-ports provide the highest output return loss and isolation while maintaining a compact size. This is achieved by employing embedded resistive films, which do not significantly enlarge the size of the compact stacked SIW concept [8]. The size difference between SP-1 and SP-2 is due to the output transitions, which for some applications may be inevitable for power detector placement and PCB layout requirements. Huebner et al. [21] presents an implementation of SP-2 including power detectors in a practical system.

Conclusion

This article presents compact K-/Ka-band multilayer, stacked SIW six-port junctions with embedded thick-film resistors. The latter improve the matching and isolation of the output ports making the six-ports robust to mismatched terminations. The two design concepts discussed differ in their output port configuration. The outputs are either stacked in pairs or located next to each other on the same layer. The latter design is based on a tailored transition and an asymmetric layer stack to equalize the amplitude balance. Measurements of the fabricated prototypes validate the concepts. The proposed six-ports are compact, fully shielded, robust to output terminations, and integrable in multilayer PCBs.

Competing interests. The authors report no conflict of interest.

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https://doi.org/10.1017/S1759078724000680 Published online by Cambridge University Press

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