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Interfaces of ZnO Nanowires Grown on Semiconducting Surfaces

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The large direct band gap of ZnO makes it an important semiconductor. ZnO can be grown in the form of nanowires on various substrates, which makes it a potential candidate for nanoparticle-based device applications such as heterojunction solar cells. Aligned nanowires of ZnO can be grown on semiconductor surfaces to make *p–n* junctions. The characteristics and performance of devices are critically dependant on the alignment, distribution and the nanowire–substrate interface character. While various methods to control the alignment and distribution of ZnO nanowire on different surfaces have been reported in the literature [1], the structure of the interface between the ZnO nanowire and the semiconducting surface is almost unknown. The motivation of this work is to characterize the interface of ZnO nanowires grown on a Si surface.

ZnO crystals were grown on a Si surface by thermal oxidation of zinc acetate. ZnO nanowires were subsequently grown using hydrothermal synthesis [2]. They were characterized using a FEI Tecnai G2 F30 TEM operated at 300 kV. The nanowires were prepared for TEM by wedge cleaving the substrate. HRTEM study of the interface was carried out on specimens prepared by conventional cross-section techniques.

Using this method, fairly dense and aligned nanowires grow on the Si surface. The nanowires are typically 100 nm in radius and about 1 μm long. Occasionally defects along the length of the nanowires can be observed. The interface between the nanowires and the Si substrate is interesting. It consists of three layers. Between the nanowires and the Si substrate a 30–40 nm-thick amorphous layer can be observed. While the interface between the nanowire and the amorphous layer is fairly flat and straight, the interface between the amorphous layer and the Si surface is not so well defined (Figure 1).

The nanowire growth on the Si substrate can be explained by the transport and dehydroxylization of the $Zn(OH)_n$ at the Si surface. The high density of the ZnO nanocrystals can be explained by the fact that ZnO nanowires can be grown without any assistance from ZnO nanocrystals. The amorphous layer is responsible for the current through the junction being about four orders of magnitude smaller than expected [3]. It is thought to be generated during the heat treatment used to generate ZnO seed nanocrystals on the Si substrate. The hexamethylenetetraamine used for the hydrothermal synthesis is also a strong oxidizer. It is believed that oxidation starts on the Si surface and the oxide interface moves into the Si substrate, which is why the interface between Si and the amorphous oxide layer is not flat, while the ZnO nanowires grow on the amorphous

oxide layer. The present study reports characterization of such nanowire–substrate interfaces. [4].

References

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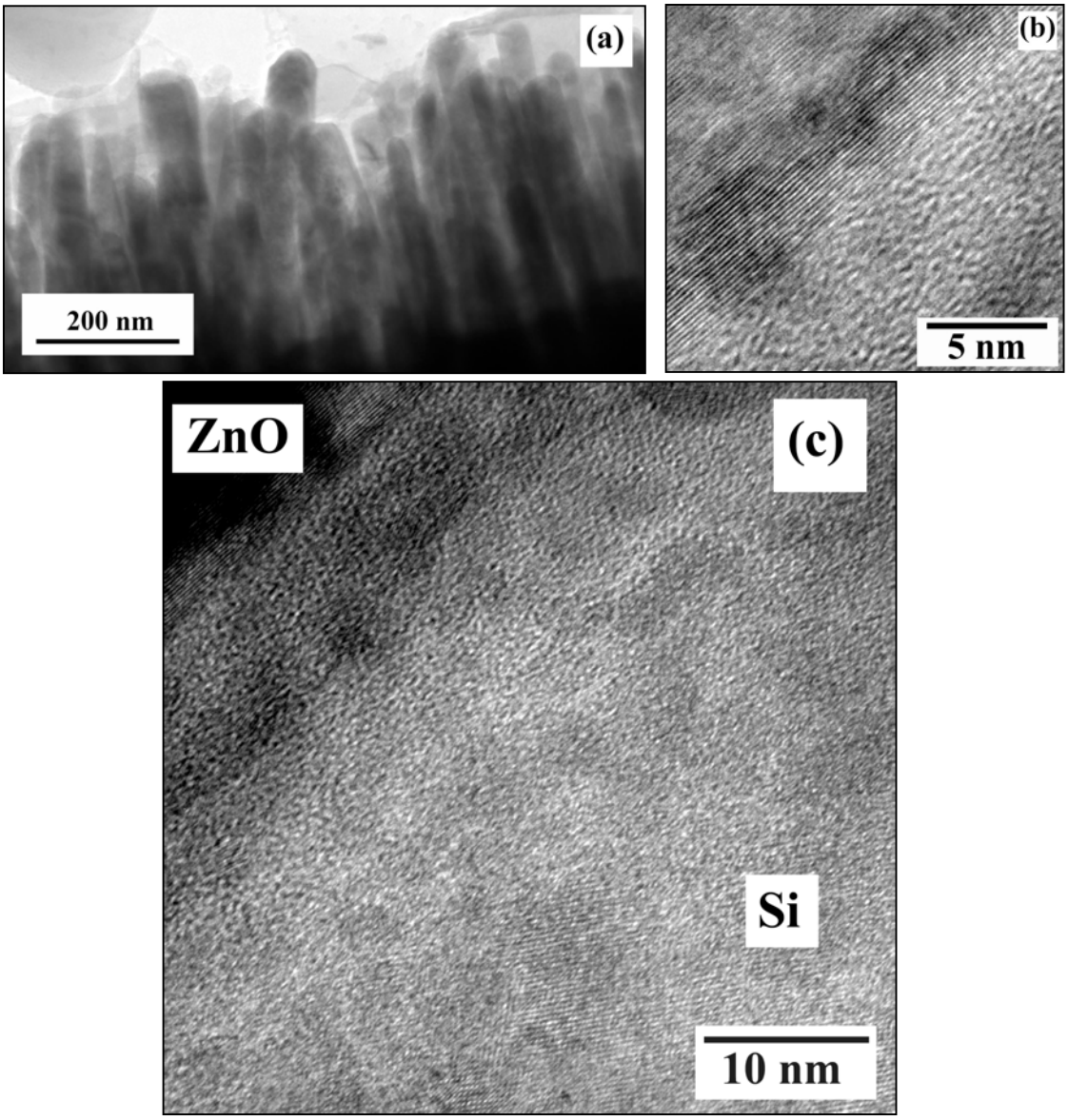

FIG. 1. (a) Overview of ZnO nanowires on a Si substrate, (b) Lattice image at the base of a nanowire. The lattice planes of the nanowire correspond to {10$\bar{1}$2}, (c) HRTEM image showing the ZnO nanowire (top left) and the Si substrate (bottom right) separated by an amorphous region.

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