doi: 10.1017/S1431927609093039
Microsc Microanal 15(Suppl 2), 2009
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Thermal Fatigue and Failure Analysis of Cu-Plated Through Hole Solder Joints

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A thermal cycle fatigue study and post-mortem failure analyses were conducted on through hole solder joints. Two types of joints were evaluated: connector-to-board and internal circuit board through holes (vias). The through hole vias in the former assemblies contain a Cu-based alloy pin, Fig. 1a, while those in the latter are either empty or solder-filled, Fig. 2a. In both assembly types, the via walls (barrels) are made from electroplated Cu. During thermal cycling, cracks develop in the Cu via walls, Figs. 1b and 2b. The thermal cycle employed was typical for assessment of high-reliability military and aerospace microelectronics, with temperature limits of -55°C and +125˚C, 15 min hold times, and ramp rates of 10°C/min. The effects of thermal cycling and partial solder filling on the propensity for Cu via cracking were investigated experimentally. The Cu fatigue cracking is caused by differential thermal expansion between the circuit board materials and the copper. Cross-sectional metallography was used to analyze the solder joints in the as-received condition and after 100, 200, 300, 500, and 1000 thermal cycles. The observations of via cracking were quantitatively summarized – the crack counting procedure is given in Ref. [1]. The phenomenon of thermal-mechanical fatigue of the Cu-plated barrels was also simulated by finite element analysis (FEA).

Optical metallography of the through hole solder joints showed that the solder was relatively free of intermetallic compound (IMC) particles on the primary side, where solder and heat were applied. Large amounts of Au-Sn IMC particles were found on the secondary side of the joints, from dissolution of Au-plated layers. Partial solder filling was attributed to this Au contamination of the solder (constitutional solidification) as well as poor flow through the thin solder gaps between the connector pins and Cu-plated vias. No Cu via cracking was observed in the as-received solder joints. *After thermal cycling, all fatigue cracks observed in the vias were associated with partial solder filling of the joints, Figs. 3a and 3b.* In general, the cracks were located at or near the solder fill level due to local strain concentration effects, Figs. 1b and 2b. The co-location of fatigue cracks and the solder fill level was predicted by FEA modeling. Acceptable agreement was also found between the FEA predicted number of cycles to failure and the experimentally observed onset of via cracking.[1]

Figures 3a and 3b show the effect of joint type on fatigue cracking tendency. For connector-to-board through holes containing a connector pin, the cracking susceptibility was less than through holes internal to the circuit boards that were empty or partially filled with solder. The Cu-alloy pin alleviates some of the mismatch in thermal expansion coefficient (CTE) since it has the same CTE as the Cu via walls. For joints that were completely solder filled, the soft solder is able to accommodate the strain built up during thermal cycling. In partially filled joints or regions with large voids in the solder, the strain becomes concentrated in the via walls due to CTE mismatch with the adjacent circuit board materials, eventually leading to cracking. For empty or solder-filled internal through holes, the absence of a Cu-alloy pin increases the cracking tendency because of greater CTE mismatch strains. This work highlights the importance of controlling soldering processes to produce joints with 100% solder filling in both connector-to-board and non-connector through hole joints.

[1] D.F. Susan, M.K. Neilsen, P.T. Vianco, and A.C. Kilgo, *Int. J Mater. and Structural Integrity*, Vol. 2, No. 1/2, pp. 138-163, 2008.
*Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the US Dept. of Energy's national Nuclear Security Administration under contract DE-AC04-94AL85000.

https://doi.org/10.1017/S1431927609093039 Published online by Cambridge University Press

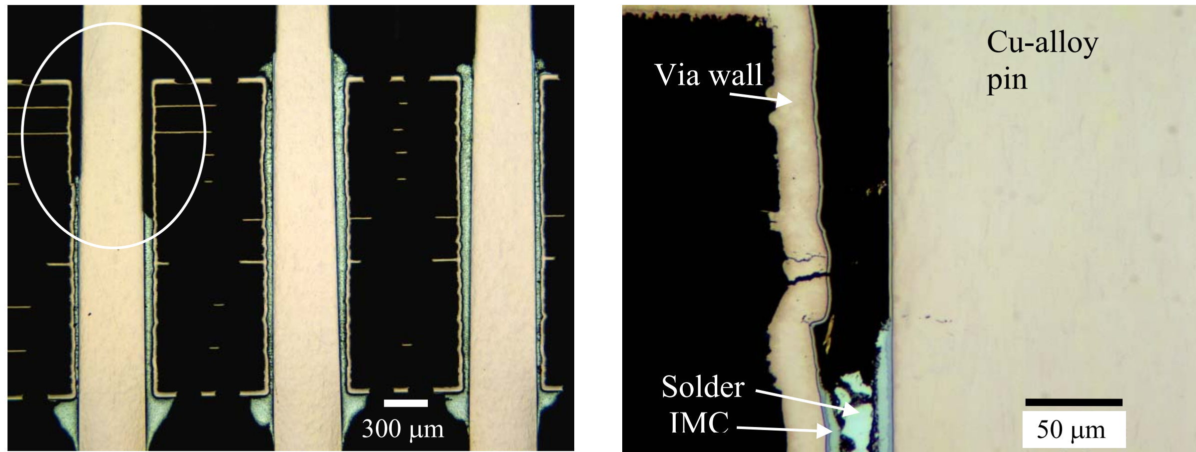

Fig. 1. a) Low magnification optical micrograph of three connector pins showing a partially filled through hole solder joint. b) Via cracks in a partially filled solder joint after 500 thermal cycles.

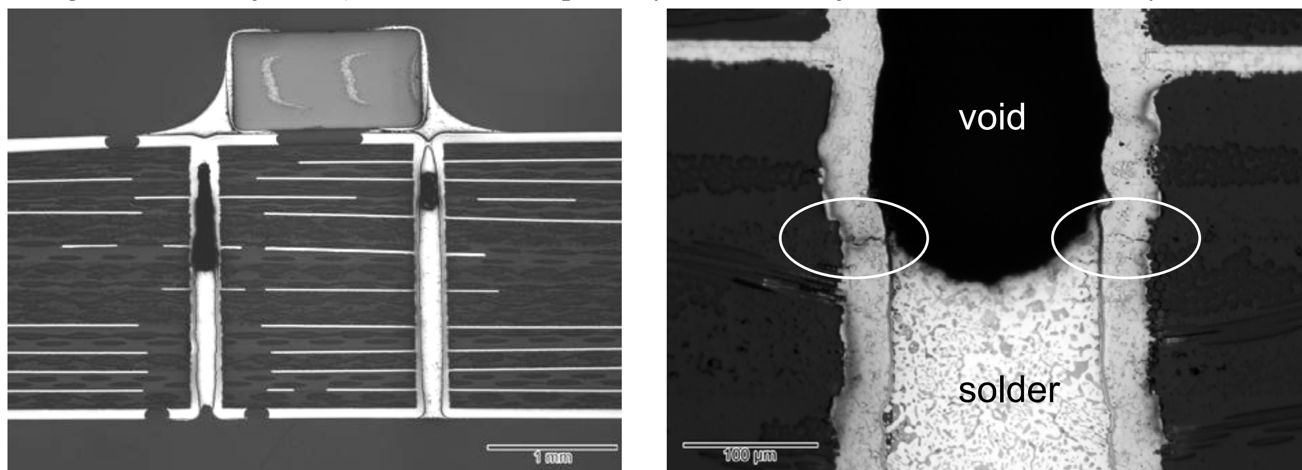

Fig. 2. a) Low magnification optical micrograph of a surface mount device with underlying solder-filled vias (no pins). b) Via cracks in a partially filled solder joint after 100 thermal cycles.

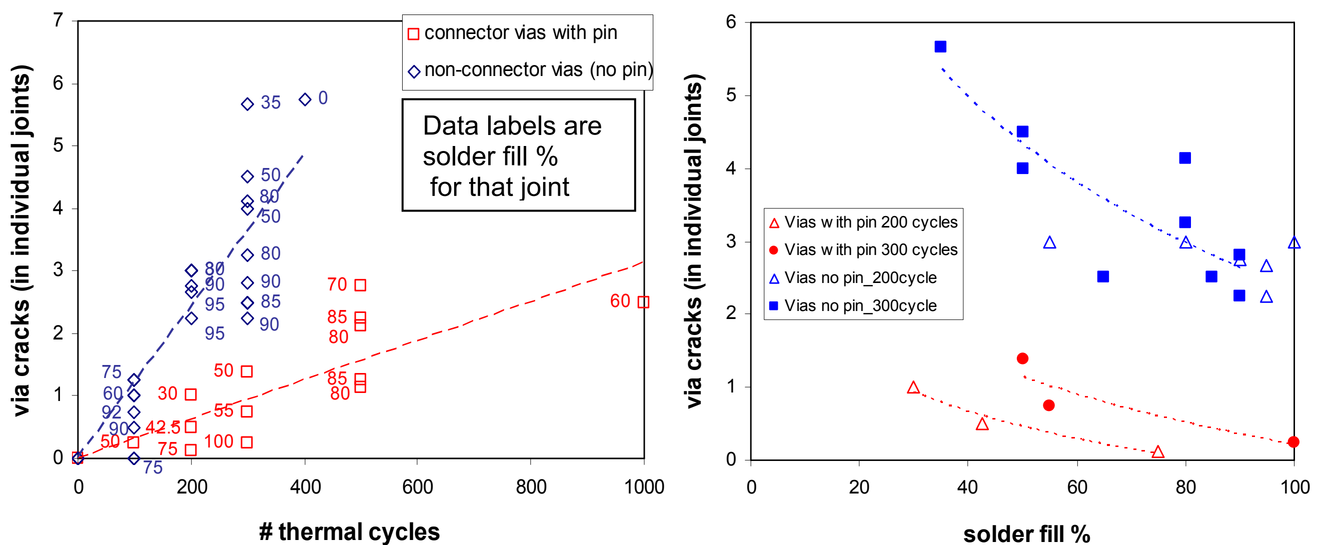

Fig. 3. a) Measured number of via cracks as a function of thermal cycling. b) Number of via cracks vs. solder fill level of individual joints for samples subjected to 200 and 300 thermal cycles.

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