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RF linearity trade-offs for varying T-gate geometries of GaN HEMTs on Si

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Research Paper

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Abstract

Short-channel Gallium Nitride (GaN) high-electron-mobility transistors (HEMTs) often utilize T-shape gates due to their large gate-line cross-sectional area and subsequent f_{MAX} increase. In this paper, we report the linearity trade-offs associated with varying the T-gate geometries of AlGaN/GaN HEMTs on Si, specifically the gate extensions which serve as field plates and their impact on the large-signal performance. Small-signal characterization and modeling, in addition to TCAD, provide initial guidelines for the optimal dimensions for the gate field plates using the ratio of f_T and the product of the gate resistance and the gate-to-drain capacitance. We utilize various characterization methods, including 6 GHz non-linear vector network analyzer characterization in addition to load-pull, to quantify the amplitude and phase distortion and their subsequent impact on the large-signal metrics of the devices under differing matching conditions and bias points. We deduce that the influence of the gate field plates on the amplitude and phase distortion is non-negligible, particularly under matched conditions.

Introduction

Modern wireless communication standards rely on spectrally efficient linear modulation techniques sensitive to amplitude and phase errors. Such standards require high linear power amplifiers (PA) in the RF front-end modules to avoid interference with the adjacent channels [1]. The well-known trade-off between efficiency and linearity, where the linearity declines at peak power efficiency, results in PA operation at backoff power levels below the maximum saturated output power (P_{SAT}) to meet the linearity specifications. Amplitude-to-amplitude (AM/AM) distortion and amplitude-dependent phase distortion (AM/PM) are known contributors to spectral regrowth, with the latter additionally causing difficulties in the received signal detection. Their combined contribution results in out-of-band interference of the transmitted signal and bit errors of the received signal [2].

Downscaled GaN HEMTs are capable of meeting the challenging output power and efficiency requirements set by modern RF and high-power applications [3]. Nevertheless, these devices are renowned for their non-linear behavior chiefly stemming from the transconductance derivatives and bias-dependent capacitances [4]. Furthermore, short-channel GaN HEMTs employ T-shape gates for a larger cross-sectional area to reduce the gate-line resistance, thereby improving the cut-off frequency of the unilateral gain (f_{MAX}). The field plates, which are connected to the gate electrically and kept at a distance above the semiconductor surface, offer a conducting plane which reduces the high electric field peaks that result in an electronic breakdown [5]. This electric field reduction at the gate edge allows the application of high voltages and subsequently higher output powers. However, their presence involves trade-offs between device parasitics, including the gate-to-drain capacitance, which influences f_{MAX} and the device linearity.

Extending our work presented in [6], we aim to provide in this paper an understanding of the trade-offs associated with T-gate geometry optimization through additional small-signal modeling and large-signal characterization. The results of the non-linear characterization of several geometrical configurations show the necessity of optimizing the gate-to-drain field plate (l_{gfp}) for an appropriate trade-off of the phase and harmonic distortion, where phase distortion is mitigated with l_{gfp} downscaling at the expense of the harmonic distortion and gain linearity.

The GaN HEMT devices

The devices under test (DUTs) are eight-finger AlGaN/GaN HEMTs fabricated in a three-level Cu damascene back end of line (BEOL) process on 200 mm Si wafers (Fig. 1) [7, 8]. The ohmic

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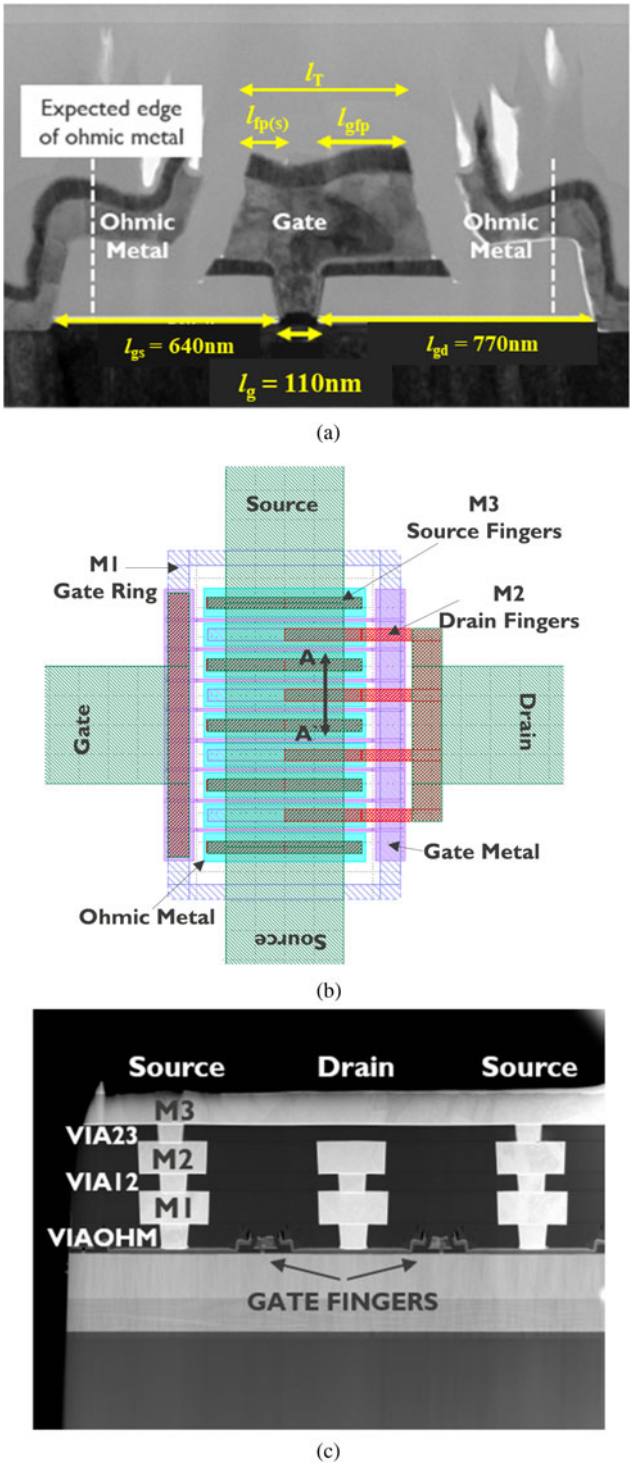

Fig. 1. (a) TEM cross-section of a 110 nm device with the definition of the dimensions. (b) Eight-finger GaN HEMT device layout with three BEOL metal layers. (c) TEM cross-section across the A-A″ cutline shown in (b) highlighting the three Cu layers.

contact resistance (R_C) is ~0.15 Ω.mm, and the sheet resistance (R_{SH}) is ~370 Ω/sq. There is an increase in the parasitic capacitance of these DUTs because the ohmic metal moved closer to the gate head than anticipated, on both the source and drain sides, during the device processing. For an 110 nm device, the maximum I_D is ~1.2 A/mm, and the peak f_{MAX} is 135 GHz, whereas this processing issue limits the peak f_T to 60 GHz (Fig. 2).

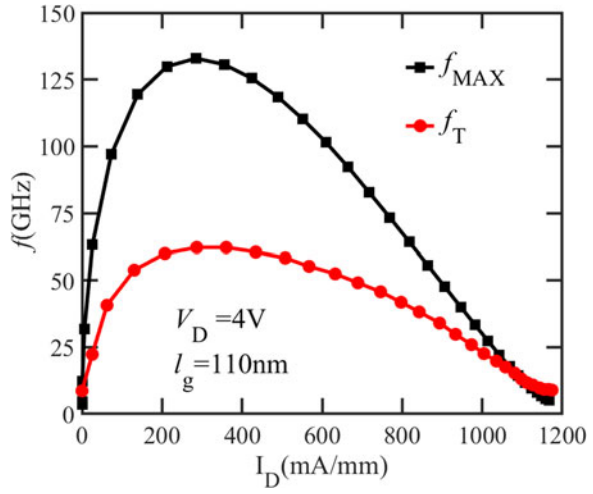

Fig. 2. f_T/f_{MAX} versus bias for the shortest device at V_D = 4 V. Device geometry: l_g = 110 nm, l_{gfp} = 250 nm, $l_{fp(s)}$ = 120 nm, l_{gs} = 540 nm, l_{gd} = 670 nm, $N_F \times W_F$ = 8 × 25 µm.

To study the impact of varying the T-gate geometries, we consider l_{gfp} ranging from 50 to 450 nm and gate-to-source field plates ($l_{fp(s)}$) of 50 and 120 nm. The downscaled gate-drain (l_{gd}) and gate-source (l_{gs}) spacings are adjusted according to the l_{gfp}, $l_{fp(s)}$ lengths to maintain a constant effective gate-to-drain and gate-to-source distances. The devices have an off-state lateral breakdown voltage (V_{BD}) of ~105 V at a breakdown criterion of 1 mA/mm.

The extrinsic transconductance (g_{me}), obtained from DC characterization, decreases with increasing the l_{gfp} (Fig. 3). This decline is due to the larger effective gate length which results in a decline in the drain saturation current in addition to the longer l_{gd} for larger l_{gfp} devices [9].

T-gate geometry: RF small-signal trade-offs

Measured *S*-parameters, using a two-port vector network analyzer (VNA), determine the small-signal device behavior. The small-signal behavior of these devices is describable by an 11-element

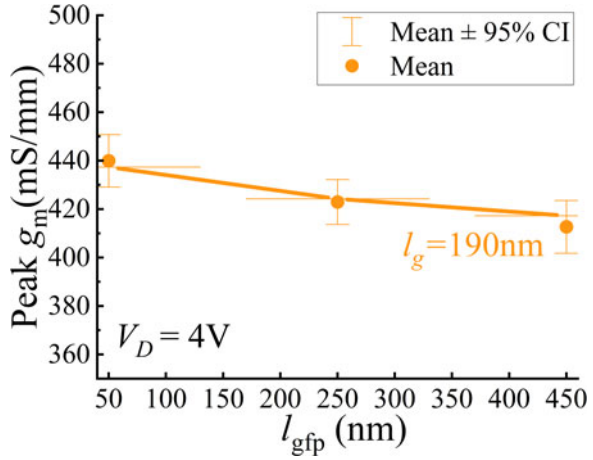

Fig. 3. Peak extrinsic transconductance for varying gate field plate lengths with error bars marking the variation across 10 measured dies at V_G set to the bias corresponding to the maximum g_m, and V_D = 4 V. Device geometry: l_g = 190 nm, l_{gs} = 220 nm, l_{gd} = 170 nm + l_{gfp}, $l_{fp(s)}$ = 50 nm, $N_F \times W_F$ = 8 × 25 µm.

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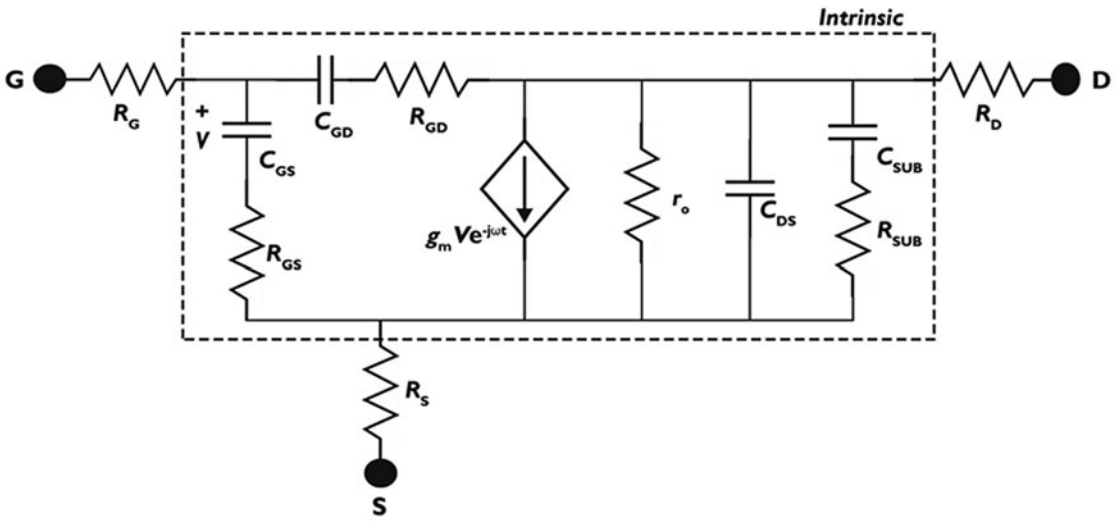

Fig. 4. Small-signal equivalent circuit used in the extraction of the intrinsic parameters and the extrinsic resistances after open-short de-embedding.

small-signal equivalent circuit (SSEC) (Fig. 4). This modeling approach is useful for identifying possible device improvements and performance limiters; particularly since the cut-off frequencies (f_T,f_{MAX}) can be approximated from the values of the equivalent circuit [10, 11]. f_{MAX} can be expressed in terms of the charging time constant $\tau_{R_GC_{GD}}$ as follows:

$$f_{MAX} = \frac{f_T}{2\sqrt{g_{ds}(R_G + R_{GS} + R_S) + 2\pi \times f_T \times \tau_{R_GC_{GD}}}} \quad (1)$$

$$f_T = \frac{1}{2\pi\tau_t} \quad (2)$$

$$\tau_t = \frac{C_{GS} + C_{GD}}{g_{m_i}}, \quad \tau_{R_GC_{GD}} = R_G C_{GD}. \quad (3)$$

Initial estimation of the values of particular parameters in the SSEC allows for validating the extraction of the small-signal parameters from the de-embedded RF measurement data. The source and drain access resistances (R_S, R_D) can be calculated from the R_{SH} and R_C, where $R_{S,D} = R_{SH}\, l_{gs,gd} + R_C$. The gate resistance ($R_G$) estimation relies on the T-gate dimensions, the gate-line sheet resistance and via resistances as detailed in [12]. A first-order prediction of the gate-to-source capacitance (C_{GS}), neglecting the fringing effect, can be deduced from the gate length and barrier thickness (T_{BAR}) using $C_{GS} = \varepsilon l_g / T_{BAR}$. Whereas the gate-to-drain capacitance (C_{GD}) should be kept at a value below 0.3 of C_{GS} in PA to limit the influence of the input Miller reflected capacitance in GaN HEMTs with scaled source-to-drain distances below 1 µm. The extraction of the parameter values for the SSEC follows the procedures in [10, 11]. The final stage of extraction validation depends on comparing the SSEC *S*-parameters and the RF measurement data (Fig. 5). The visible kink in S_{22} (Fig. 5) is an indicator of the parasitic conduction through the Si substrate, and the SSEC accounts for this effect through the $R_{SUB}C_{SUB}$ branch (Fig. 4) [13, 14]. The work in [15, 16] provides

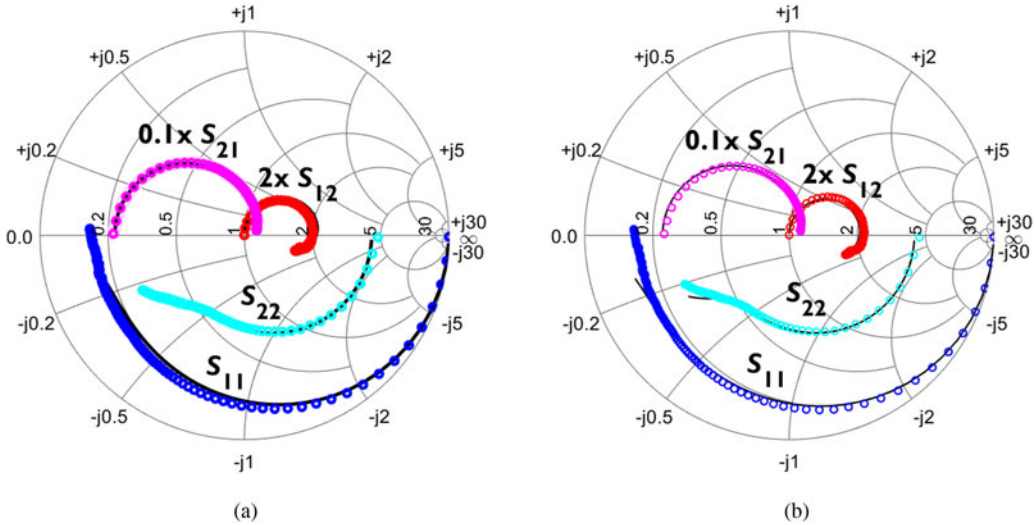

Fig. 5. Measured (symbols) versus modeled (lines) *S*-parameters with a frequency ranging from 100 MHz to 50 GHz at $V_D = 4$ V and V_G set to maximum g_m. Device geometry: $l_g = 190$ nm, $N_F \times W_F = 8 \times 25$ µm, $l_{gs} = 220$ nm, $l_{gd} = 170$ nm + l_{gfp}, $l_{fp(s)} = 50$ nm, and l_{gfp} = (a) 50 nm, (b) 250 nm.

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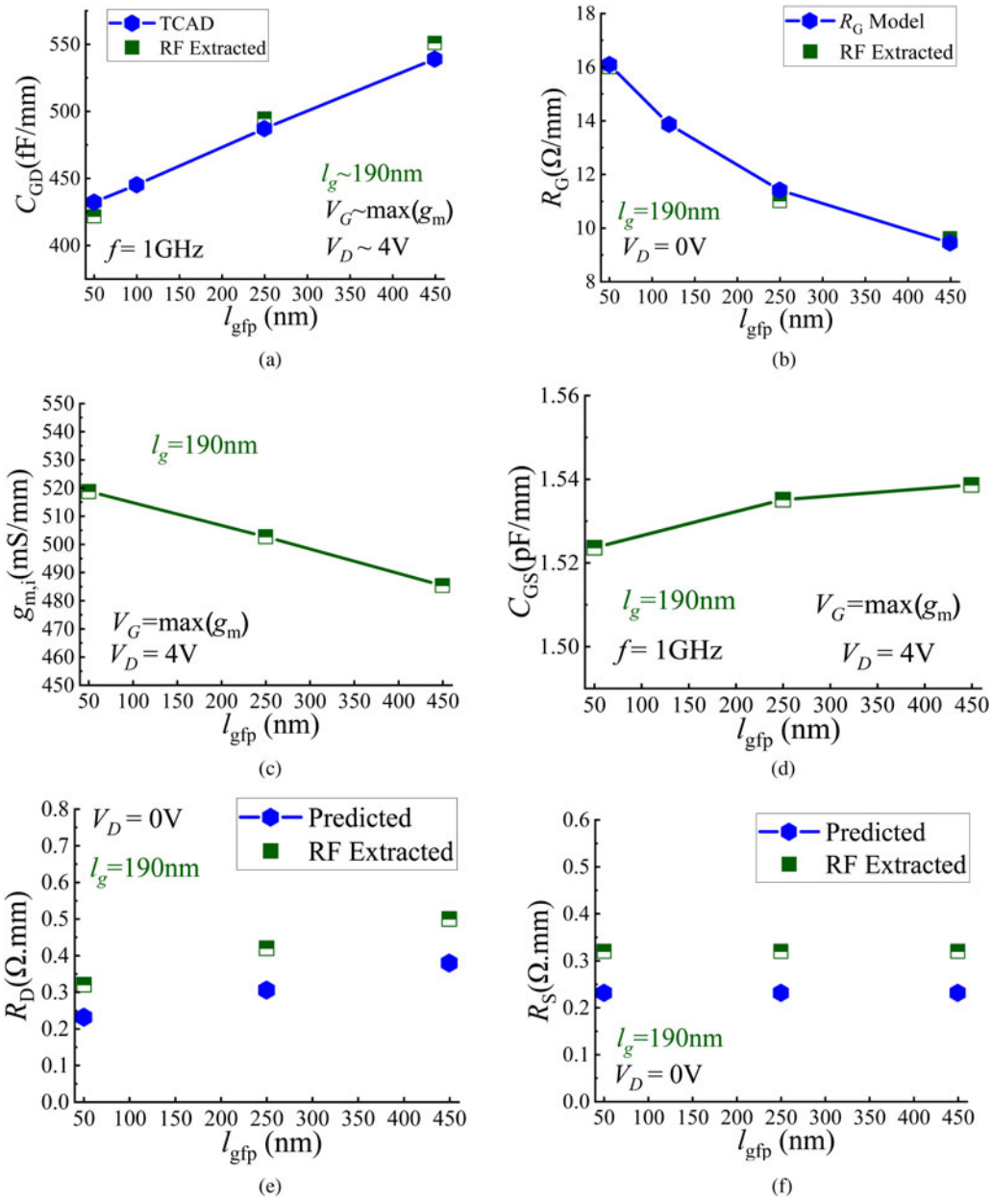

Fig. 6. Extracted and predicted small-signal parameters for three different l_{gfp}. Device geometry: l_g = 190 nm, l_{gs} = 220 nm, l_{gd} = 170 nm + l_{gfp}, and $N_F \times W_F = 8 \times 25$ µm. The remaining SSEC parameters with marginal l_{gfp} dependence: C_{DS} = 495 fF/mm, r_o = 900 Ω/mm, and C_{SUB} = 50 fF, R_{SUB} = 250 Ω.

further insight into the substrate-related RF losses and non-linearities for these GaN HEMTs on Si.

The sharp increase in R_G (Fig. 6(b)) as the l_{gfp} reduces to 50 nm causes a consequent decline in f_{MAX} (Fig. 7(b)) even though f_T (2) (Fig. 7(a)) continues to improve with smaller l_{gfp} due to the consistent increase in the intrinsic transconductance (g_{mi}) (Fig. 6(c)) and capacitance reduction (Figs 6(b) and 6(d)). Variation in the l_{gfp} dimensions results in a trade-off between R_G and C_{GD} [12]. Assuming negligible l_{gfp} influence on the ratio between the output and input device impedance[1] in the formulation for f_{MAX}, the time constant $\tau_{R_G C_{GD}}$ (Fig. 8(a)) can be used as an initial design guideline for l_{gfp} optimization.

[1]The ratio between the output and input device impedance refers to the term $g_{ds}(R_G + R_{GS} + R_S)$.

Technology Computer-Aided Design (TCAD) device simulations performed using the Sentaurus Device software enable additional validation of the extracted C_{GD}, where the TCAD GaN HEMT structure is generated using the Sentaurus Structure Editor software [17, 18]. The TCAD simulations include the drift-diffusion model for carrier transport and Fermi statistics. Additionally, the mobility model incorporates the doping-dependent and high-field saturation dependency. The built-in strain piezoelectric polarization model automatically computes the polarization charges at interfaces [17, 19]. The model coefficients have been carefully calibrated based on measurements of different GaN devices. The simulations also include the bulk and interface traps.

Using the R_G model in [12] and the TCAD simulations to explore more l_{gfp} geometries, it is observable that the parabolic

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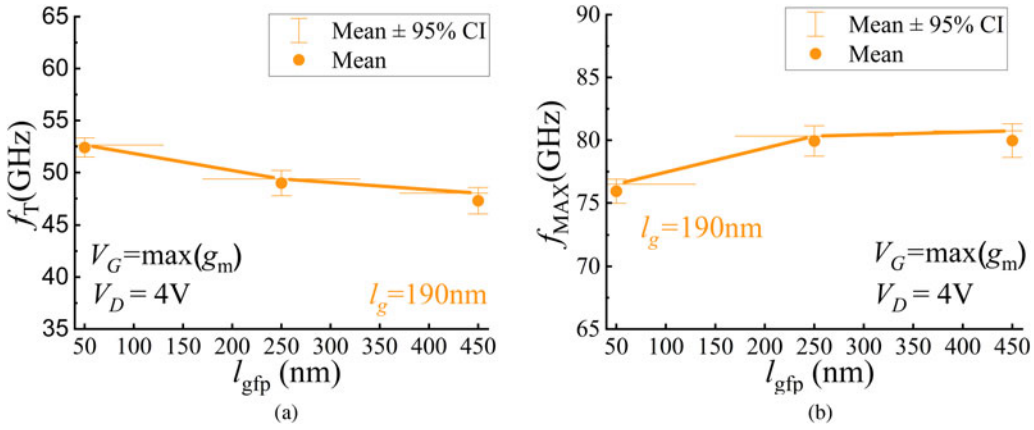

Fig. 7. (a) f_T and (b) f_{MAX} for varying gate field plate lengths with error bars marking the variation across 10 measured dies at V_G set to the bias corresponding to the maximum g_m, and V_D = 4 V. Device geometry: l_{gs} = 220 nm, l_{gd} = 170 nm + l_{gfp}, $l_{fp(s)}$ = 50 nm, and $N_F \times W_F$ = 8 × 25 µm.

ratio between f_T and $\tau_{R_G C_{GD}}$ has an optimum beyond which its value declines. In the case of small l_{gfp}, the decline is a result of a rise in R_G, and for larger l_{gfp}, it is a consequence of an increase in C_{GD} coupled with a lower g_m. There is no impact of l_{gfp} variation on the R_S (Fig. 6(f)). However, the direct proportionality between R_D and the l_{gfp} captures the influence of the gate-to-drain field plate (Fig. 6(e)).

As discussed in the next section, the l_{gfp} can be optimized further for linearity; since the voltage-dependent C_{IN} results in an amplitude-dependent phase shift which affects AM/PM. Longer l_{gfp} exhibit a higher capacitance variation for a given V_G range ($\partial C_{IN}/\partial V_{GS}$) (Fig. 8(b)), thereby negatively affecting the phase distortion.

Non-linear characterization

Measurement setups

This study relies on three different setups which enable the non-linear and large-signal device characterization to examine various metrics at different fundamental frequencies. The non-linear vector network analyzer (NVNA), previously described in [6], provides non-linear device behavior insight at a fundamental frequency (f_0) of 6 GHz under unmatched conditions (50 Ω) with the harmonics acquired up to 18 GHz ($3f_0$) [20]. The frequency specifications of some setup components, such as the pre-amplifier and the coupler, limit the acquisition of higher-order harmonics. The matched large-signal performance of the devices is measured using passive continuous-wave load-pull setups calibrated at 6 and 28 GHz (Fig. 9). Load-pull measurements rely on controlling the reflection factor (𝕣) presented to the device, which is the ratio of the reflected power to the injected power wave into the load [21]. In passive load-pull measurements, the transmission losses and the tuner reflection capacity limit the achievable loads; hence the 𝕣 is always less than 1, rendering all the achievable impedances inside the smith chart. The losses of the coupler, connected between the tuner and the DUT, limit the 𝕣 to 0.69 (voltage standing wave ratio (VSWR) ~ 5.6) in the 6 GHz setup. In the 28 GHz load-pull measurement setup, the tuner is connected directly to the probe, thereby enabling a high 𝕣 of 0.891 (VSWR ~ 17.4). Rigorous calibration moves the reference plane to the tip of the 100 µm-pitch ground-signal-ground (GSG) probes. The devices are biased in the frequently preferred class AB since this class offers advantages in terms of linearity and efficiency when compared to classes B and A, respectively [22]. This study considers two bias conditions; a mid-class AB bias point, consistent with the NVNA results presented in [6], at a current density of 320 mA/mm, and a deep class-AB bias at 60 mA/mm.

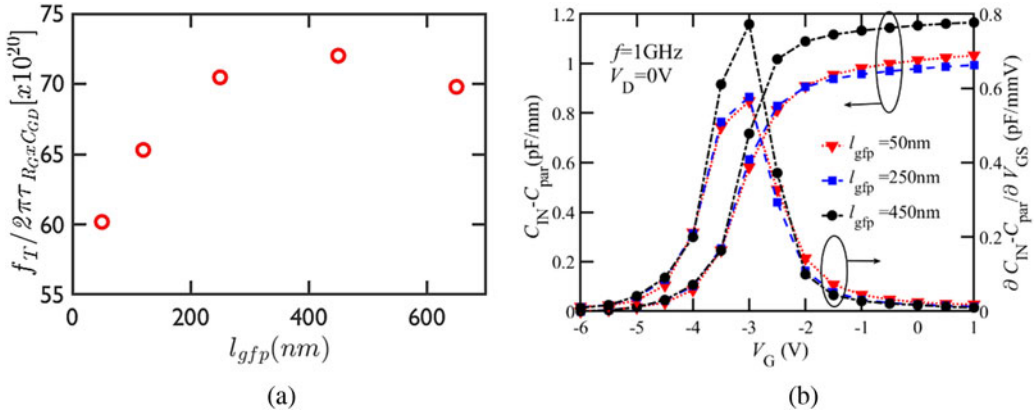

Fig. 8. (a) The ratio between f_T and the product of R_G and C_{GD} extracted from R_G modeling and TCAD simulations. (b) C_{IN}–$C_{parasitic}$, and $\partial C_{IN}/\partial V_{GS}$ versus V_G for varying l_{gfp}. l_g = 190 nm, l_{gs} = 220 nm, l_{gd} = 170 nm + l_{gfp}, and $N_F \times W_F$ = 8 × 25 µm.

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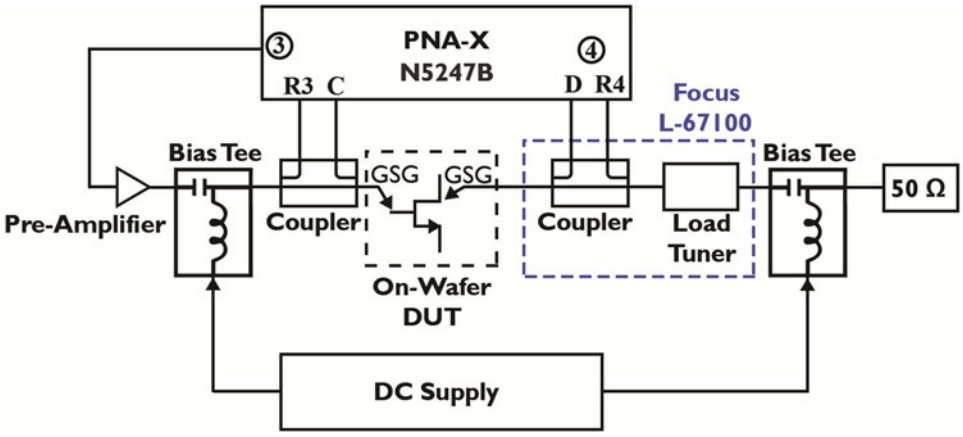

Fig. 9. Passive load-pull characterization setup with the Focus L-67100 Delta Tuner. Achieved VSWR: 17.4 (Γ: 0.891), characterization frequency $f = 28$ GHz.

Amplitude and phase distortion

Since GaN HEMTs show soft-compression behavior, the input power level that results in the peak power-added efficiency (PAE) and P_{SAT} is at approximately 3 dB of compression [23]. Hence, the maximum phase distortion reported, computed from the difference between the phase of the measured *B2* and *A1* waves, is at P_{SAT}.

$$AM/PM = Phase(B2_{f0}) - Phase(A1_{f0}). \quad (4)$$

The reduction of the l_{gfp} results in mitigation of the AM/PM (Figs 10 and 11) owing to the lower $\partial C_{IN}/\partial V_{GS}$ for the smallest l_{gfp} (Fig. 8(b)) [6]. The larger the rate of change of the capacitance fluctuates for a given V_G range ($\partial C_{IN}/\partial V_{GS}$), the higher the phase distortion [23–25]. The discussion of the impact of the matching conditions and operating frequency on the distortion will follow.

Although the impact of gate-to-drain capacitance (C_{GD}) variation with the excitation amplitude on AM/PM is negligible, there is an influence of the input Miller reflected C_{GD} on AM/PM. Such Miller capacitances are dependent on the non-linear voltage gain (A_v) of the device, their loop gain ($1 - A_v$) accordingly varies at the onset of gain compression [26, 27].

The linearity of the transconductance profile in the region where I_D is in saturation is critical at high input power levels. The g_m roll-off of GaN HEMTs results in the gain compression and worsens the linearity in the P_{SAT} regime. The non-linear access resistance is a known contributor to this g_m roll-off, and its impact increases with direct proportionality to the drain current because of the rise of the electric field in the access region. Since the area below the field plate acts as a transition between the non-linear access region and the intrinsic device, it similarly influences the g_m roll-off.

There is consistent direct proportionality of l_{gfp} and AM/PM at different matching conditions (Fig. 10), operating frequencies, and bias points (Fig. 11). A 120 nm gate-to-source field plate, $l_{fp(s)}$, results in a 22% increase in AM/PM compared to a 50 nm $l_{fp(s)}$ (Fig. 11), implying that the $l_{fp(s)}$ has a similar impact on AM/PM as the l_{gfp}. These findings infer that the optimal gate field plate extension lengths for linearity within the optimal range, defined in section "T-gate geometry: RF small-signal trade-offs," are dependent on the target application. Shorter lengths are the recommended topology for phase distortion-sensitive applications at low voltage operation to maintain a sweet-spot balance of gain, AM/AM and AM/PM.

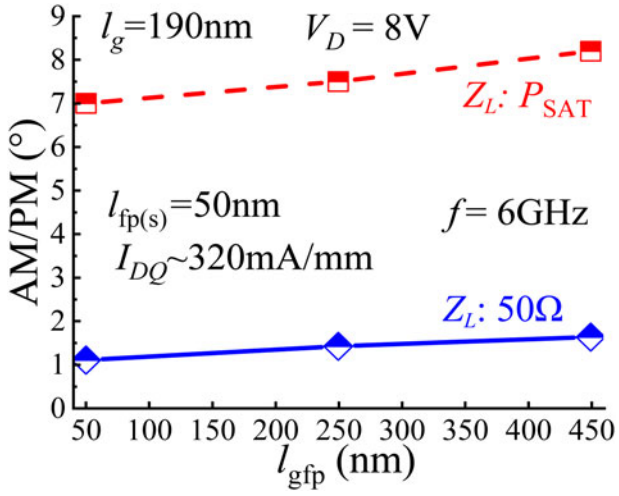

Fig. 10. Phase distortion characteristics at 6 GHz for differing l_{gfp}, at unmatched (NVNA) and matched (load-pull) load conditions with $I_{DQ} = 320$ mA/mm and $V_D = 8$ V. $l_g = 190$ nm, $l_{gs} = 220$ nm, $l_{gd} = 170$ nm + l_{gfp}, $l_{fp(s)} = 50$ nm, and $N_F \times W_F = 8 \times 25$ µm.

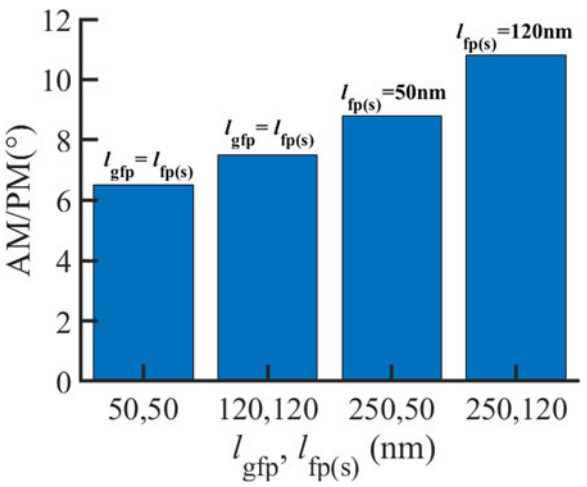

Fig. 11. AM/PM characteristics obtained from the 28 GHz passive load-pull characterization for varying l_{gfp}, $l_{fp(s)}$ at $I_{DQ} = 60$ mA/mm and $V_D = 4$ V. $l_g = 190$ nm, $l_{gs} = 170$ nm + $l_{fp(s)}$, $l_{gd} = 170$ nm + l_{gfp}, and $N_F \times W_F = 8 \times 12.5$ µm. Z_L is matched for PAE.

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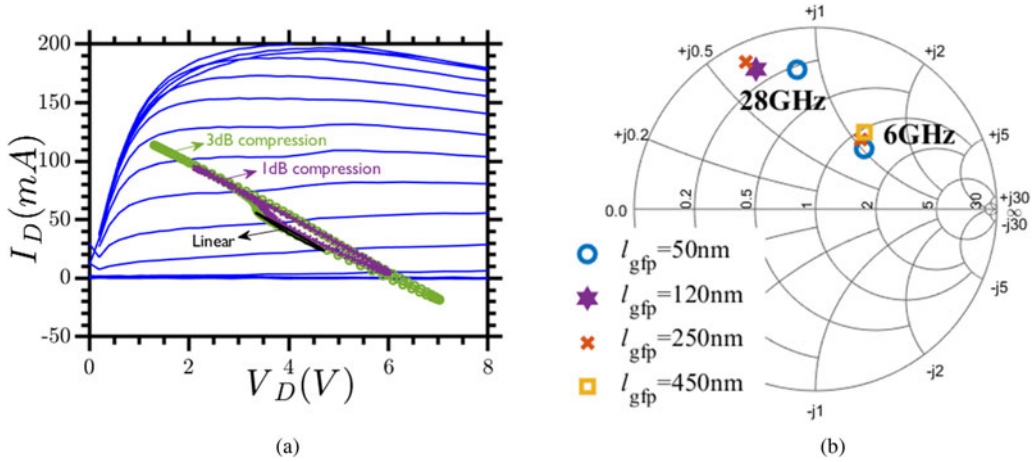

Fig. 12. (a) Dynamic load lines, obtained from 6 GHz NVNA characterization at different compression levels, superimposed upon the DC characteristics, $N_F \times W_F = 8 \times 25$ µm, $l_{gfp} = l_{fp(s)} = 50$ nm, V_G ranges from −6 to 0.8 V with a 0.4 V step and $I_{DQ} = 200$ mA/mm, $V_{DQ} = 4$ V. (b) PAE optimal load points obtained from load-pull characterization at 6 and 28 GHz for varying l_{gfp}. $l_g = 190$ nm.

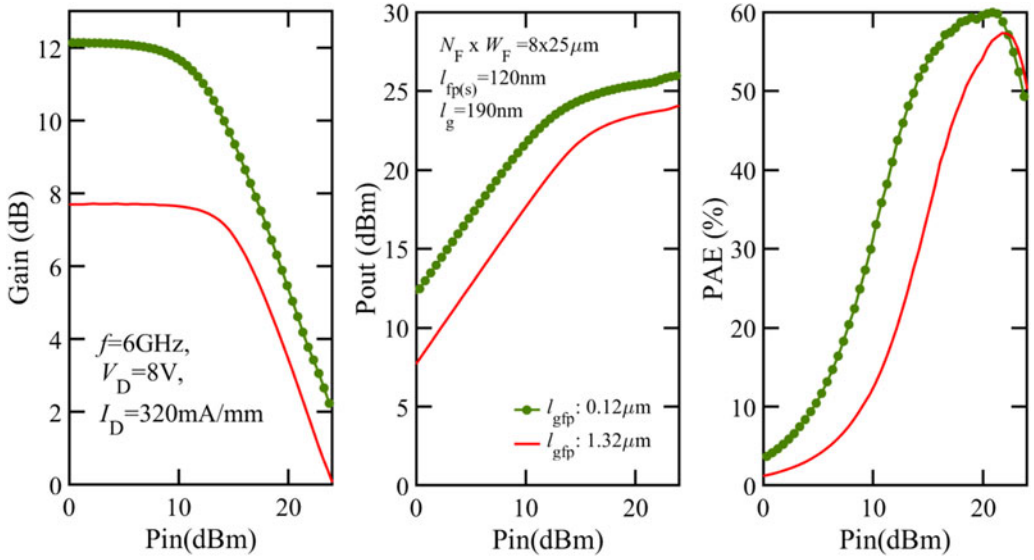

Fig. 13. Large-signal metrics versus P_{IN} obtained from the 6 GHz passive load-pull characterization for varying l_{gfp} at $I_{DQ} = 320$ mA/mm and $V_D = 8$ V. $l_g = 190$ nm, $l_{gs} = 540$ nm + $l_{fp(s)}$, $l_{gd} = 540$ nm + l_{gfp}, $l_{fp(s)} = 120$ nm, and $N_F \times W_F = 8 \times 25$ µm.

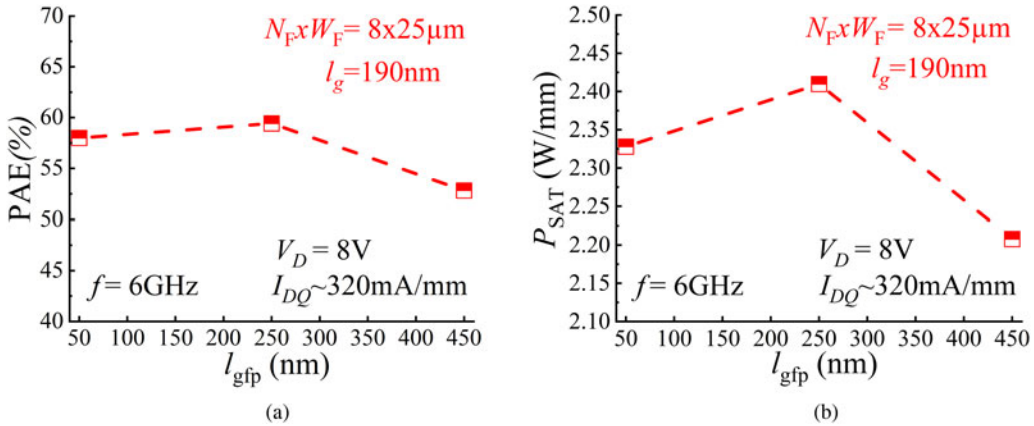

Fig. 14. Median PAE, P_{SAT} obtained from the 6 GHz passive load-pull characterization of three dies for varying l_{gfp} at $I_{DQ} = 320$ mA/mm and $V_D = 8$ V. $l_g = 190$ nm, $l_{gs} = 170$ nm + $l_{fp(s)}$, $l_{gd} = 170$ nm + l_{gfp}, $l_{gfp} = 50$ nm, and $N_F \times W_F = 8 \times 25$ µm.

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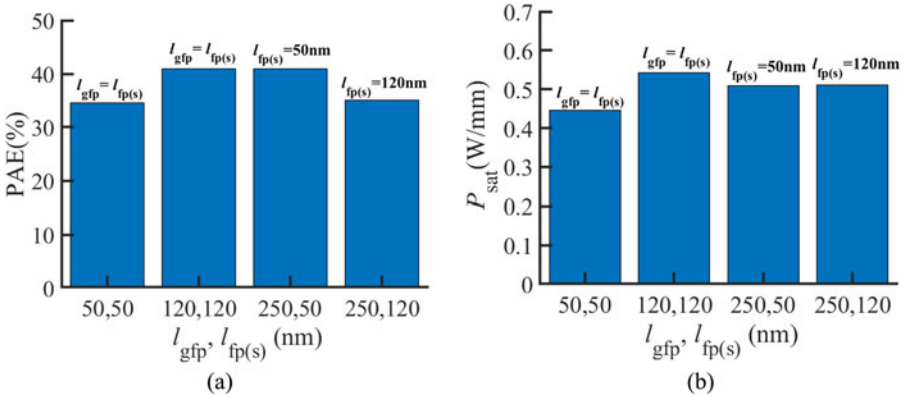

Fig. 15. Peak PAE, P_{SAT} obtained from the 28 GHz passive load-pull characterization varying l_{gfp}, $l_{fp(s)}$ at I_{DQ} = 60 mA/mm and V_D = 4 V. l_g = 190 nm, l_{gs} = 170 nm + $l_{fp(s)}$, l_{gd} = 170 nm + l_{gfp}, and $N_F \times W_F = 8 \times 12.5$ µm.

Presenting the device with a matched load raises the value of the distortion (Fig. 10). In single-stage PAs, this impact of a matched reactive load on AM/PM is linked to implicit non-linear feedback through the reverse current of the device from the drain voltage phase to the drain current phase [26]. The need for inductive tuning for device matching is due to the capacitive nature of the device, which results in an elliptical dynamic load-line (Fig. 12(a)) [5]. The dynamic load-line shifts and extends outside the DC IV characteristics as the device is pushed further into compression. The average RF current value also increases, which results in the commonly observed rise in I_D at higher input power levels. The network capacitance rises further as the device is pushed into saturation, necessitating inductive tuning (Fig. 12(b)) for matched conditions where the device delivers peak RF performance. The change in the optimal load impedance with the operating frequency explicates the difference in AM/PM values at 6 and 28 GHz (Fig. 12(b)).

Large-signal metrics

Following the g_m and f_T trends, the 6 GHz load-pull characterization under matched conditions for l_{gfp} of 120 nm and 1.32 µm shows a reduction in the device power gain for the longer l_{gfp} leading to a lower P_{SAT} and PAE (Fig. 13). The PAE continues to improve with decreasing the l_{gfp} until it saturates for lengths between 250 and 50 nm. The P_{SAT} follows the same direction until it declines for a 50 nm l_{gfp} (Fig. 14). Performing load-pull at 28 GHz leads to similar observations (Fig. 15). Varying the $l_{fp(s)}$ shows a decline in PAE for the longer 120 nm length. To optimize the T-gate geometry for low-voltage ($V_D < 10$ V) mm-wave operation and considering the previous findings with regards to the device gain, AM/AM, AM/PM, and large-signal performance, the smallest feasible l_{gfp} is the recommended choice in the range where the ratio between f_T and $\tau_{R_G C_{GD}}$ does not sharply decline.

Conclusion

This optimization study of T-gate geometries for linearity and improved large-signal performance indicates an optimum range for the gate field plate extension lengths for downscaled devices targeting mm-wave operation. The ratio of f_T and the product of gate resistance and gate-to-drain capacitance defines this optimum, thus accounting for the sharp increase in gate resistance with aggressively downscaled gate field plates. Within that optimal range, a symmetric T-gate with a smaller gate field plate is ideal for phase distortion-sensitive applications since we find that AM/PM is inversely proportional to the gate field plate length in consequence of the direct proportionality between phase distortion and capacitance. This T-gate configuration provides the best trade-off for gain and phase linearity, thus improving the large-signal performance metrics, PAE, and P_{SAT}.

Conflict of interest. None.

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