DESIGN AND RELIABILITY ASSESSMENT OF NOVEL 3D-IC PACKAGING

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ABSTRACT

Presently, physical limitations are restricting the development of the microelectronic industry driven by Moore's law. To achieve high-performance, small form factor, and lightweight applications, new electronic packaging methods have exceeded Moore's law. This research proposes a double-chip stacking structure in an embedded fan-out wafer-level packaging with double-sided interconnections. The overall reliability of the solder joints and redistributed lines is assessed through finite element analysis. The application of soft lamination material and selection of a carrier material whose coefficient of thermal expansion (CTE) is close to that of the printed circuit board can effectively enhance the reliability of solder joints over more than 1,000 cycles. A trace/pad junction whose direction is parallel to the major direction of the CTE mismatch is recommended, and the curved portion of trace lines can absorb the expansion of metal lines and filler material. Design-on-simulation methodology is necessary to develop novel packaging structures in the electronic packaging industry.

Keywords: Fan-out wafer-level packaging, Finite element analysis, Life prediction model.

1. INTRODUCTION

In recent years, consumer electronic products have evolved to have characteristics of light weight, high capacity, and high efficiency. The development of the microelectronic industry is driven by Moore's law [1], which has predicted over the past 45 years that the number of transistors on an IC chip will double every 24 months. However, physical limitations are present in the complementary metal-oxide semiconductor (CMOS) processing technology. The future development of electronic packaging will be achieved by the more than Moore's law [2]. Existing functions can be integrated using system-in-package (SiP) approaches, such as three-dimensional integrated circuit (3D-IC) packaging, 3D-IC integration, and 3D Si integration [3], by stacking in a vertical direction to avoid physical limitations in the CMOS process. Through silicon via (TSV), the core technique of both 3D-IC and 3D Si integration, is used to interconnect stacked chips, thereby enhancing perfor-mance, shortening signal transmission time, and solving signal delay issues. By contrast, fabrication cost and TSV yield remain as critical issues obstructing the application of chip-stacked-type packaging in consumer electronic products. 3D-IC packaging executed by the package-on-package (PoP) method is an adequate solution to accomplish the SiP approach. This technique also satisfies the demands for high performance, short signal transmission, and heterogeneous integration [4].

In the most common PoP stacking configuration, several package approaches, including wire bonding, flip-chip, and ball grid array (BGA), are stacked [5]. Global chip trends have developed toward a smaller chip area with an increasing number of interconnections. The shrinkage of the pitch of the pads on the chip side is significantly faster than that on the substrate side [6]. This situation can be considered as an interconnection gap. Infineon Technologies AG [7] has developed a fan-out wafer-level ball grid array (WLB), called embedded WLB (eWLB), that can solve interconnection gaps. In

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an eWLB configuration, the chip is smaller than the package; hence, the additional packaging area can provide space for the increasing number of interconnections. Yew *et al*. [8] developed the chip-on-metal wafer-level chip scale package (CSP) technology with fan-out capability. The reliability characteristic was described using finite element (FE) analysis, and it was concluded that a thinner chip, superior trace scheme, and application of a suitable stress buffer layer could decrease the stress/strain value in the redistribution layer (RDL). The same team also proposed a panel base package (PBP) technology with fan-out capability to expand the fine pitch input/output (I/O) of chips using the RDLs on the applied soft filler material [9]. The FE analysis showed that the reliability of solder joints was enhanced by soft lamination materials and filler polymers. Therefore, metal line failure is the major reliability concern resulting from large deformations produced by thermal cycling.

Infineon [10] has claimed a semiconductor device that includes a semiconductor chip embedded by encapsulation material, which has TSVs and through molding vias (TMVs) extending through the semiconductor chip and encapsulation material, respectively. The structure also includes double-sided interconnections that can fulfill PoP stacking. National Tsing Hua University [11,12] invented a structure in which the first and second electronic devices are stacked, and they are embedded in a chip carrier. Conductive vias in the carrier connect the first and second electronic devices.

In the present research, a double-chip stacking structure in an embedded fan-out wafer-level packaging (WLP) with double-sided interconnections is proposed, as shown in Fig. 1. As techniques in microelectronic processing progress, ultrathin chips can be produced successfully. The thickness of a double-sided WLP with double-chip stacking structure can be controlled to within 500 μm. The proposed structure involving the development of heterogeneous integration technology, multiple functions, and different-sized dies can be incorporated into a single packaging unit interconnected through lateral RDLs and vertical TMVs. The present study assessed the reliability issue of solder joints, copper traces, and copper vias remaining in the novel 3D-IC packaging structure due to its large size and complicated structure. A FE analysis was performed that incorporated the Coffin-Manson relation and Engelmaier model to predict the fatigue life of solder joints and conducted traces, which was validated through experiments. Structure design and material selection were also studied through FE analysis.

2. PROCESS FLOW FOR DOUBLE-SIDED WITH DOUBLE-CHIP STACKING STRUCTURE

The detailed manufacturing process of the double-sided with double-chip packaging structure is shown in Fig. 2. The fabrication of this stacking structure can be completed by a semiconductor processing-compatible technology and achieved through either wafer-level or panel-level processes. First, through carrier vias (TCVs) are formed in the carrier wafer through laser drilling and electroplating processes. The material selected for the carrier is silicon to enhance heat dissipation and the stiffness of the packaging structure. The copper is the first Cu trace layer is also plated onto the silicon car-
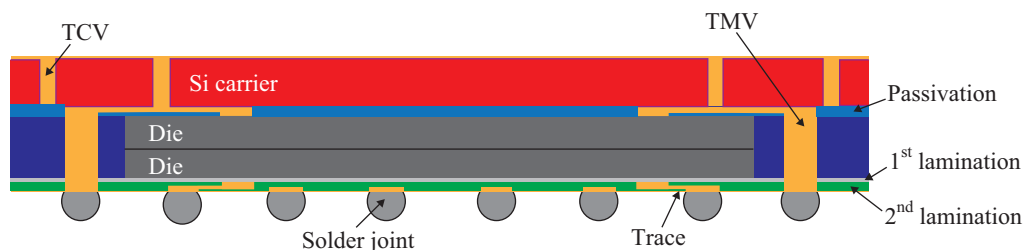

Fig. 1   Schematic of the double-sided with double-chip packaging structure.
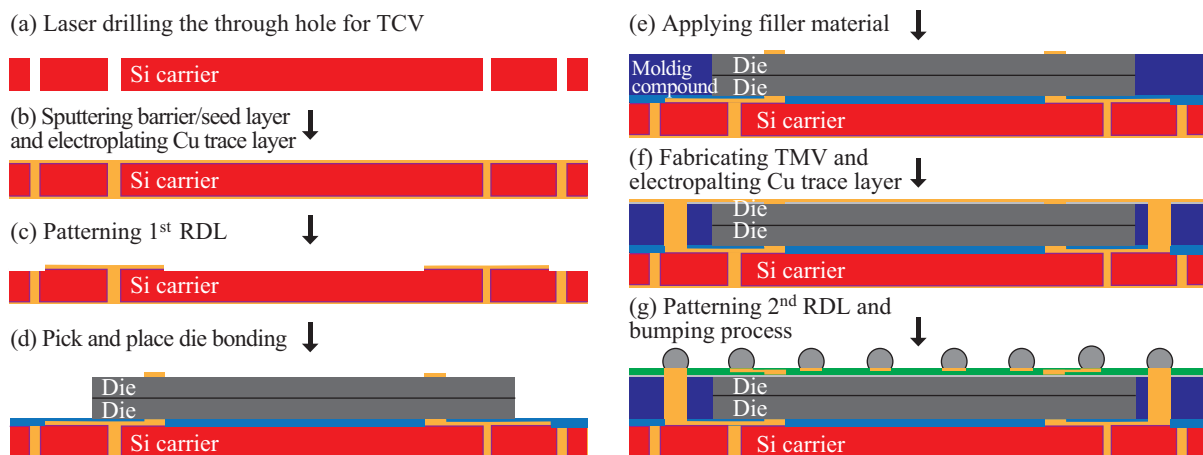

Fig. 2   Process flow for the double-sided with double-chip packaging structure.

rier. Then, the copper is etched following the RDL layout formed on the mask.

At the same time, the dies are thinned to almost 50 μm, and the back sides of the two thinned dies are bonded with an adhesive film after functional testing is performed. The stacked dies are picked and placed on the silicon carrier wafer, which has a bigger area to form a reconstituted wafer, and the dies are bonded with the first RDL. An example of stacked dies rearranged on the silicon carrier is shown in Fig. 3. The dies are then encapsulated by using molding compound to broaden the
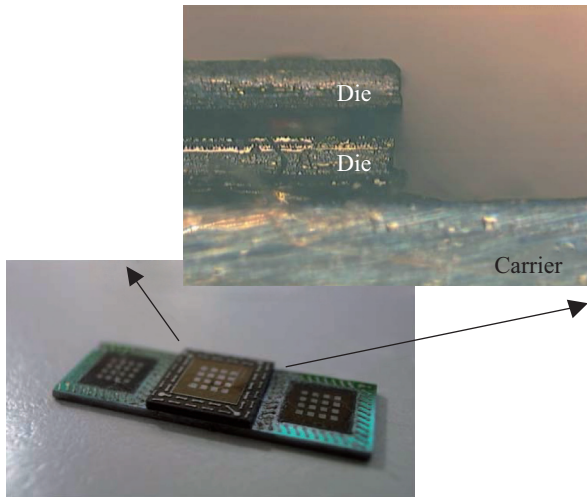

Fig. 3   Sample of stacked dies arranged on the silicon carrier (Source: ITRI).

package area, thereby providing additional base material when proceeding with the second RDL and TMVs. The first lamination layer is coated onto the surface of the reconstituted wafer. TMVs are formed in the periphery of the molding compound through laser drilling and

copper plating processes. Also, the copper traces are electroplated onto the first lamination layer to form the second RDL by the same process used with the first RDL. The electrical I/Os and TMVs are interconnected through RDLs; I/Os are thus re-routed from the dies to the molding compound to ensure a coarse pitch. Then, the second lamination layer is coated onto the second RDL for protection. Finally, a standard bumping process, which includes solder joint placement and reflow, is performed. After the bumping process, the reconstituted wafer is diced into numerous packaging units.

3. FUNDAMENTAL THEORY

3.1 Prediction of Solder Joint Thermal Fatigue Life

As electronic products are subjected to temperature loading during the service period, the solder joint can undergo significant nonlinear thermal stress/strain related to low-cycle fatigue. Interconnections such as solder joints and trace lines are the main locations of fatigue failure in electronic packaging. The empirical Coffin-Manson relation based on plastic strain has been extensively used to assess the reliability of solder joints [13-15] and is described as follows:

$$N_f = C(\Delta\varepsilon_{eq}^{pl})^{-\alpha} \tag{1}$$

where N_f is the mean cycle to failure, and $\Delta\varepsilon_{eq}^{pl}$ is the incremental equivalent plastic strain, which means that the solder joints in advance packaging, such as WLP and flip chip, would be subjected to each directional stress during thermal loading. The incremental equivalent plastic strain per cycle ($\Delta\varepsilon_{eq}^{pl}$) is defined as:

$$\Delta\varepsilon_{eq}^{pl} = \frac{\sqrt{2}}{3}\sqrt{(\Delta\varepsilon_x^{pl} - \Delta\varepsilon_y^{pl})^2 + (\Delta\varepsilon_y^{pl} - \Delta\varepsilon_z^{pl})^2 + (\Delta\varepsilon_z^{pl} - \Delta\varepsilon_x^{pl})^2 + \frac{3}{2}\Delta\gamma^{pl}} \tag{2}$$

where $\Delta\varepsilon_x^{pl}$, $\Delta\varepsilon_y^{pl}$, and $\Delta\varepsilon_z^{pl}$ are the incremental plastic strain along the x, y, and z directions, respectively, and $\Delta\gamma^{pl} = \Delta\gamma_{xy}^{pl2} + \gamma_{yz}^{pl2} + \gamma_{zx}^{pl2}$, where $\Delta\gamma_{xy}^{pl}$, $\Delta\gamma_{yz}^{pl}$, and $\Delta\gamma_{zx}^{pl}$ are the respective incremental plastic shear strains at the xy, yz, and zx planes. In Eq. (1), the fatigue ductility coefficient (C) and the fatigue ductility exponent (α) for the eutectic solder are 0.4405 and 1.96, respectively. These values depend on the solder materials used. In this research, the maximum equivalent plastic strain after one cycle is obtained through FE analysis and is substituted into the modified Coffin-Manson relation to predict the fatigue life of solder joints for reliability assessment.

3.2 Prediction of Trace Line Thermal Fatigue Life

In addition to the solder joints, the trace lines also suffer from cyclic loading, which induces considerable thermal stress/strain during operation. The cumulative stress/strain may damage the interconnection lines and induce fatigue failure of the electronic packaging. In WLP, a stress buffer layer is developed under the solder joints to enhance their reliability. When using a soft material with huge deformation, the reliability of the trace lines near the stress buffer layer is another issue in advanced packaging. Engelmaier proposed a new ductility and flexural fatigue testing method for copper foil and flexible printed wiring [16, 17]. This method is

also applied to predict the fatigue life of copper alloys with commonly available tensile properties. The Engelmaier fatigue model is as follows:

$$\Delta\varepsilon = \Delta\varepsilon_e + \Delta\varepsilon_p = 0.9\frac{S_u}{E}\left[\frac{\exp(D_f)}{0.36}\right]^{-0.1785\log(10^5/N_f)} + D_f^{0.75}N_f^{-0.6}$$

(3)

where E is Young's modulus, S_u is the ultimate tensile strength and D_f is the fatigue ductility. As previously mentioned, plastic strain dominates the low-cycle fatigue region, whereas elastic strain is significant in the high-cycle fatigue region. Fatigue life in the low-cycle range is only dependent on fatigue ductility. The Engelmaier fatigue model was originally applied to determine the fatigue ductility of copper foil given the fatigue life, cyclic strain, and tensile properties. Moreover, if the fatigue ductility of copper foil, the cyclic strain and tensile properties are known, fatigue life can also be predicted using the Engelmaier model.

4. VERIFICATION OF FINITE ELEMENT ANALYSIS

A 3D FE model of traditional WLP for a 256-MB DDR SDRAM [18] is first constructed to validate the accuracy of the simulation procedure and to achieve the suitable mesh density for the solder joint. Traditional WLP consists of a silicon die, copper pad, polyimide stress buffer layer, solder mask, and solder joint, as depicted in Figs. 4 and 5. The die size is 6.6 mm × 12 mm × 500 μm. The pad opening on the die side is 380 μm, and that on the substrate side is 340 μm. The traditional WLP has 52 solder joints, which include 4 dummy balls
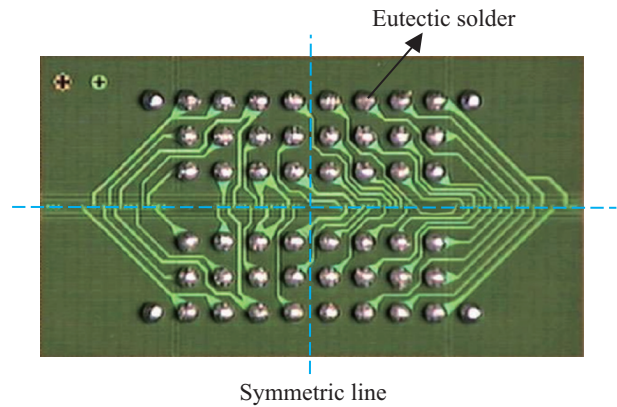

Fig. 4 Top view of the tradition WLP sample.

on the corners. This structure indicates that the daisy chain circuit interconnects 48 solder joints, and the other 4 solder joints are considered as structural supporters. Due to the symmetrical characteristic of the structure, the quarter FE model is established, and symmetric boundary conditions are applied to the symmetric planes. All materials in the traditional WLP are assumed to be isotropic and linearly elastic except for the eutectic solder joint, which is considered as a temperature-dependent and elastic-plastic material, as shown in Table 1 and Fig. 6. The with temperatures ranging from -40°C to 125°C following the JEDEC standard (JESD22-A104-B, condition G) [19]. The stress-free temperature is set to 25°C. The simulation results show that the maximum incremental equivalent plastic strain after 5 cycles is 1.97%, and the fatigue life of the solder joint predicted by the Coffin-Manson relationship is 968 cycles. The Weibull distribution of the solder joint during thermal cycling testing is shown
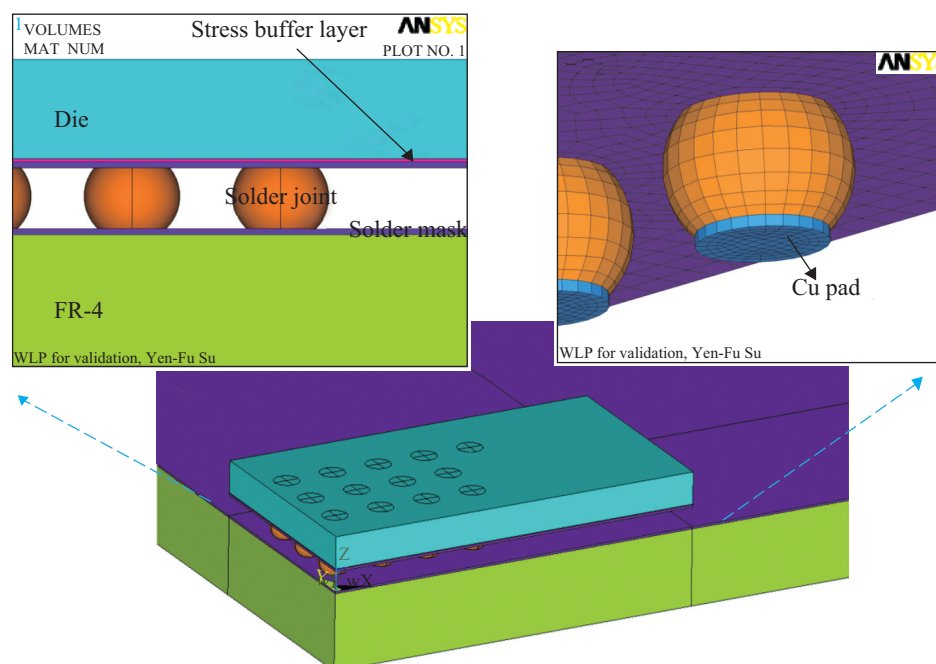

Fig. 5 The quarter FE model of the traditional WLP.

in Fig. 7 [18]. The mean cycles to failure indicate a failure probability of 63.2% in 1,007 cycles. Therefore, the simulation result is in accordance with the experimental data. The analytical procedure and mesh density of the solder joint are adopted in the following research.

Table 1 Material property used in the traditional WLP.

Material	Young's modulus (GPa)	Poisson's ratio	CTE (ppm/°C)
Silicon	169.2	0.28	2.62
Copper pad	68.9	0.34	16.7
Solder mask	3.5	0.35	30
FR-4 substrate	18	0.19	16
Polyimide	2.8	0.34	50
63Sn/37Pb	nonlinear	0.35	23.9
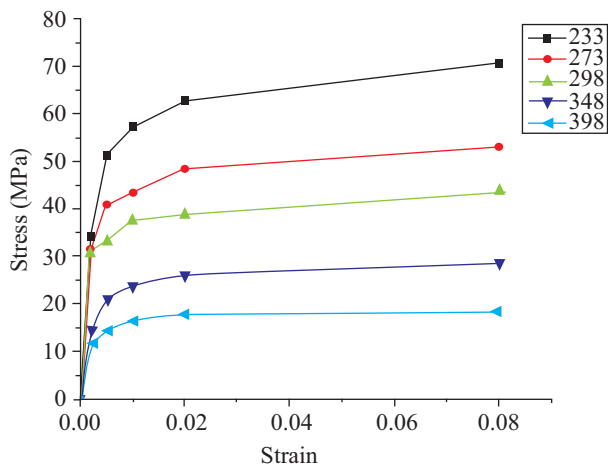
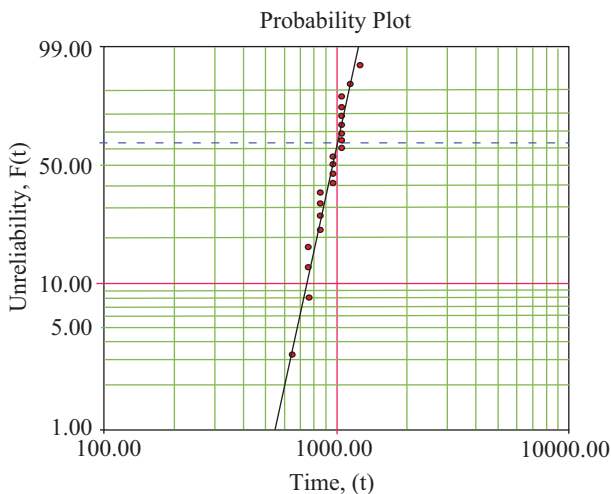Fig. 6 The temperature-dependent non-linear material property of eutectic solder.

Fig. 7 Weibull distribution of the traditional WLP failures.

5. FINITE ELEMENT ANALYSIS OF DOUBLE-SIDED WITH DOUBLE-CHIP STACKING STRUCTURE

5.1 Finite Element Modeling of Double-sided with Double-chip Stacking Structure

Before the double-sided with double-chip stacking structure begins to be manufactured, the actual mechanical behavior during thermal cycling loading and reliability assessment should be analyzed. Given the symmetrical characteristic, the quarter FE model of the proposed structure with detailed RDLs is established by use of the commercial software ANSYS®, as shown in Fig. 8(a). To assess the reliability of trace lines in the proposed structure, detailed first and second RDLs are considered, as shown in Fig. 8(b). All main components are included in the FE model, which is composed of stacked dies, adhesive film, molding compound, lamination layer, copper pad, trace lines, copper vias, passivation layer, TMV, silicon carrier, solder joints, and the printed circuit board (PCB), as shown in Fig. 8(c). The solder joint profile is predicted by using the surface evolver, and the pad openings on the chip side and PCB side are 200 μm. The solder joints are arranged in a 6 × 6 array within the chip area, and 16 solder joints are arranged along the periphery of the package. A dummy solder ball is located at each of the four corners. The pitch of the solder joint is 800 μm.

The simulation procedure and the suitable mesh density for the solder joints has been validated through traditional WLP and thermal cycling tests. In addition, the thickness and width of the trace lines are 15 μm and 40 μm, respectively, and the mesh density refers to previous research, which has validated the trace line with a thermal cycling test [9]. A 96.5Sn/3.5Ag lead-free solder is used in the proposed structure, and the related material properties are shown in Table 2. The temperature-dependent non-linear material properties of this solder and the electroplating copper are shown in Figs. 9 and 10, respectively. In the board-level analysis, the established FE model is subjected to thermal cycling loading with temperatures ranging from -40°C to 125°C to investigate the thermal-mechanical behavior of the redistribution lines.

5.2 Reliability Assessment and Failure Mechanism

The equivalent plastic strain pattern of the solder joints after one simulation cycle is shown in Fig. 11(a). The maximum equivalent plastic strain in the proposed structure occurs on the outermost solder joints at which the distance from the neutral point is the largest. However, the outermost solder joints on the corners are used to design the bypass trace line for a daisy chain circuit, so the current does not flow through them in a real device. These solder joints can be regarded as the dummy balls. Thus, the reliability assessment focuses on the solder joints other than the dummy balls. As shown in Fig. 11(b), the maximum equivalent plastic strain on the solder joints, excluding the dummy balls, occurs on the corner of the solder joints within the chip region after
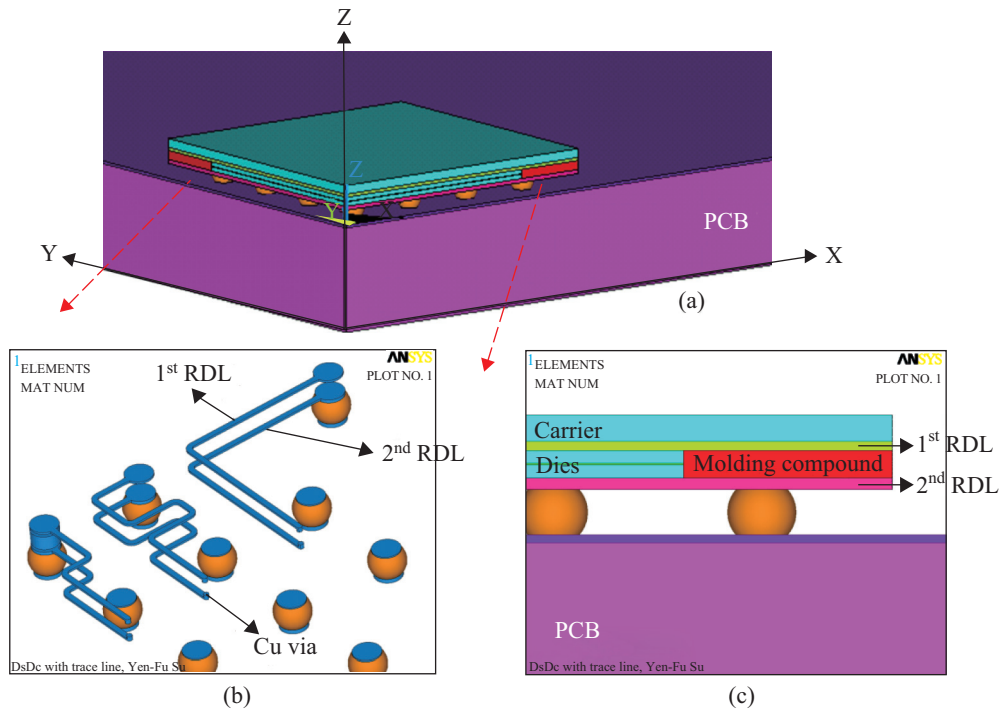
Fig. 8 FE model with detailed redistribution layers (a) overview; (b) trace lines structure; (c) cross-section.

Table 2 Material property used in the proposed structure.

Material	Young's modulus (GPa)	Poisson's ratio	CTE (ppm/°C)
Silicon	169.2	0.28	2.62
Molding compound	14.21	0.3	13
Copper	nonlinear	0.34	16.7
Solder mask	3.5	0.35	30
PCB	18.2	0.3	16
Lamination	0.09	0.41	150
Adhesive	0.05	0.4	167
96.5Sn/3.5Ag	nonlinear	0.4	22.36
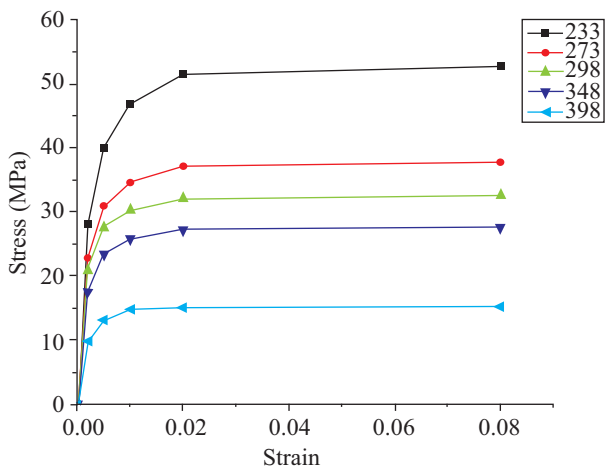
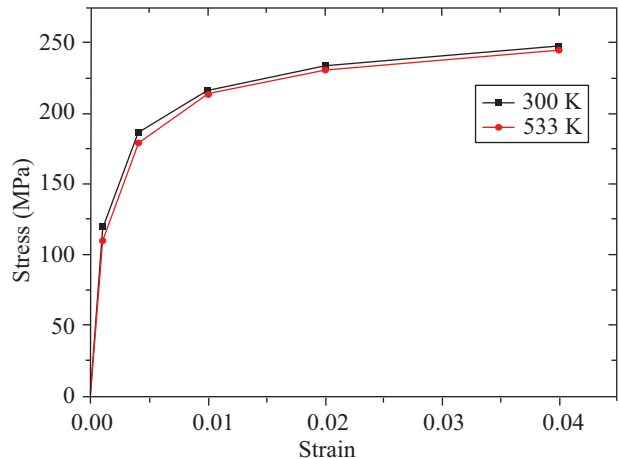Fig. 9 The non-linear material property of 96.5Sn/3.5Ag solder.

Fig. 10 The non-linear material property of electroplating coppe.

one cycle. After five thermal cycle computations, the incremental equivalent plastic strain of the solder joints converges to 0.64%. According to the Coffin-Manson relation, the mean cycle-to-failure of the solder joint is predicted to be approximately 8,633 cycles. The coef-

ficient of thermal expansion (CTE) mismatch would induce both out-of-plane and in-plane deformations at the same time. However, the application of a soft lamination layer could absorb the energy acting on the solder joints by acting as a stress buffer layer through which the thermal stress/strain can be easily released by deformation of the soft pad constrain. As a result, the fatigue lifetime of the solder joint passes the standard that electronic industries follow.
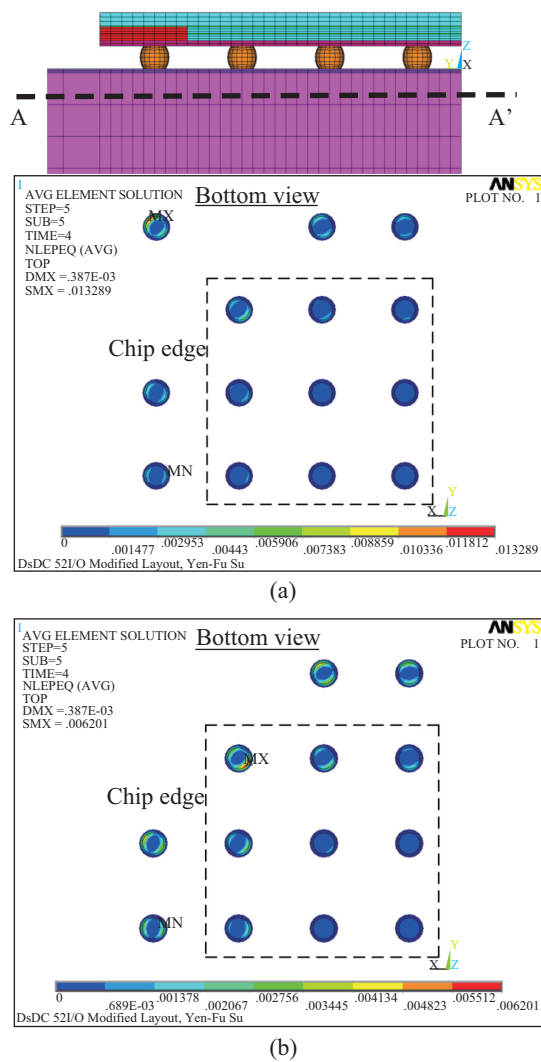

(a)

(b)

Fig. 11 The equivalent plastic strain pattern of the solder joints (a) with dummy ball; (b) without dummy ball.

In contrast, after the applied temperature loading, the concentration of stress and strain occurs at three positions along the redistribution line, the copper via, the trace/pad connecting junction, and the right angle of the metal line, as shown in Fig. 12. The dashed line represents the positions of the un-deformed state. The out-of-plane movement not only pushes the pads upward, but the in-plane deformation induced by the CTE mismatch between the package and the PCB also extends the metal lines. The maximum total strain range of the second RDL including the elastic and plastic terms is 0.89% at the via. Comparing the Engelmaier's round-robin experiment and the thermal cycling test, half of the

total strain range is applied in Eq. (3). In addition, S_u/E, computed as 1.731×10^{-3}, is obtained through the standard tensile test of copper, and the fatigue ductility (D_f) used in Engelmaier model is 0.172, as determined by Yew [20]. The predicted fatigue life of trace layer is 2,819 cycles.
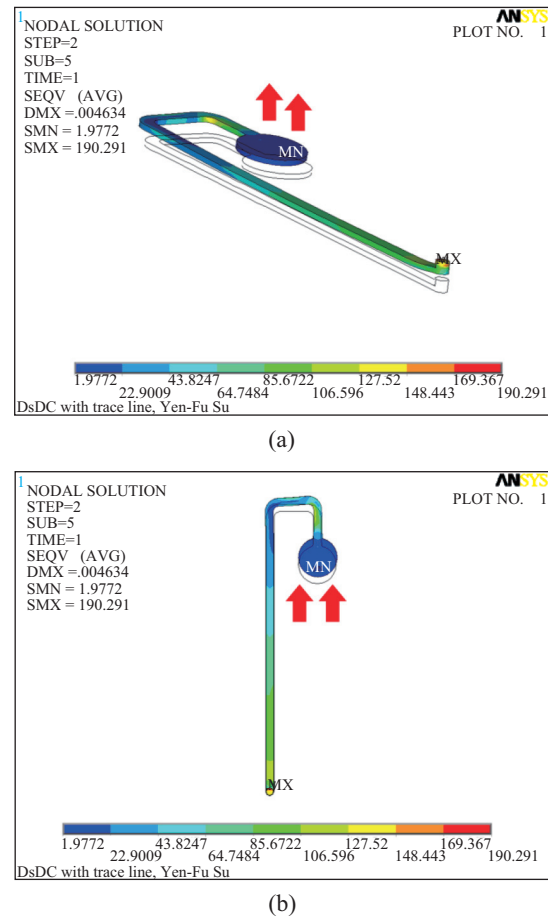

(a)

(b)

Fig. 12 Deformed metal line of the second RDL at 125 °C (a) oblique view; (b) top view (scale factor = 15)

6. PARAMETRIC ANALYSIS

6.1 Effects of Stress Buffer Layer

The effect of the stress buffer layer in the proposed structure is investigated by adjusting the thickness of the first lamination layer, as shown in Fig. 1. The baseline model is composed of the first lamination layer with a thickness of 20 μm, which was chosen from a range of thickness of 5 to 40 μm. In the fabrication process, its thickness can be controlled with the spin-coating recipe by adjusting the spin speed and time. The results indicate that the equivalent plastic strain increases significantly as the thickness of the lamination layer decreases, especially for the dummy balls, as shown in Fig. 13. Although the reliability of the solder joints will worsen as the thickness of lamination layer decreases to 5 μm, the predicted life is still higher than 2,000 cycles.
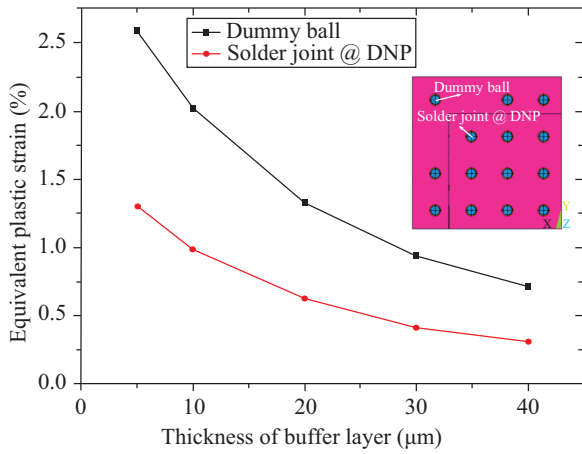
Fig. 13 Equivalent plastic strain under different thickness of buffer layer

The material selected for the lamination layer in the baseline model is SINR^{TM} polymer material, with a Young's modulus of only 0.09 GPa. However, polyimide is the most common material used as a stress buffer layer in traditional WLP. To be compatible with available processing technology in the electronic packaging industry, polyimide is also applied as a lamination layer and investigated through FE analysis. The comparison of material properties between SINR^{TM} and polyimide is shown in Table 3. From the results, the equivalent plastic strain value of a signal joint increases to 1.75% as the polyimide is applied, as shown in Fig. 14. This can be explained by the stiff lamination material, which constrains the solder joints and results in the deformation of the solder joints along with CTE mismatch. However, the predicted life cycle from the empirical relation is still more than 1,200 cycles, and thus its reliability can pass the standard that most electronic industries follow.

Table 3 Material selection for lamination layer.

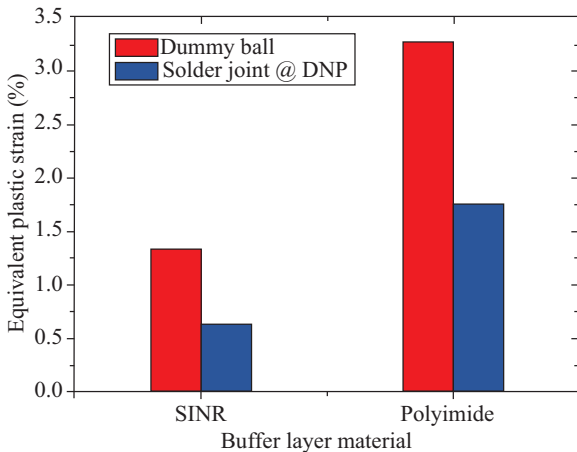| Modified material	Young's modulus (GPa)	Poisson's ratio	CTE (ppm/^{o}C)
SINR	0.09	0.41	150
Polyimide	2.8	0.34	20

Fig. 14 The effect of material selection of buffer layer.

6.2 Effects of Carrier Material

CTE mismatch between the silicon carrier and molding compound can produce out-of-plane deformation at the package level, whereas CTE mismatch between the package unit and the PCB can cause in-plane deformation at the board level. The proper selection of carrier material can reduce out-of-plane or in-plane deformation, so it is also a critical issue in the design of the proposed structure. The selected material in the baseline model is silicon, and it is replaced by ceramic and glass substrates. The material properties of silicon, ceramic, and glass are listed in Table 4. Figure 15 shows the maximum equivalent plastic strain on the dummy balls and that the signal joints are obviously dropped as the carrier material is adjusted. This can be explained by the use of the selected ceramic and glass whose CTEs are close to that of the PCB (16 ppm/°C), so the in-plane movement induced by the CTE mismatch between the carrier and PCB can be reduced.

Table 4 Material selection for carrier.

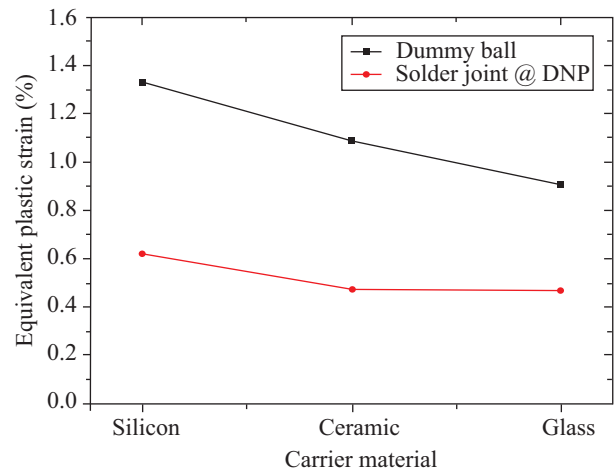| Modified material	Young's modulus (GPa)	Poisson's ratio	CTE (ppm/oC)
Silicon	169.2	0.28	2.62
Ceramic	300	0.25	8
Glass	71.5	0.21	8.14

Fig. 15 The effect of material selection of carrier.

6.3 Effects of Trace Direction

Two groups of RDLs are designed to study the effects of trace direction and curved structure. Five metal lines are designed to simulate the effect of trace direction, and they connect to pads from 90° to 270°, as shown in Fig. 16. From the simulation results, the strain values of the first RDL do not vary along with the trace direction no matter what filler material is used, as shown in Fig. 17(a). However, Fig. 17(b) shows that the predicted strain values are clearly altered among metal lines of the second

200

RDL. The direction of the trace/pad junction at 135°, 180°, and 225° is perpendicular to the major direction of the CTE mismatch, and the extension of the metal line is seriously constrained at the junction. The direction of the junction at 90° and 270° shows better performance, and it is recommended in the double-sided with double-chip stacking structure.
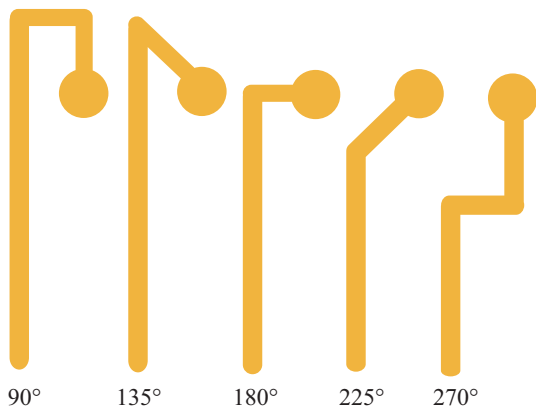

Fig. 16 Breakdown drawing of designed redistribution lines for trace direction.
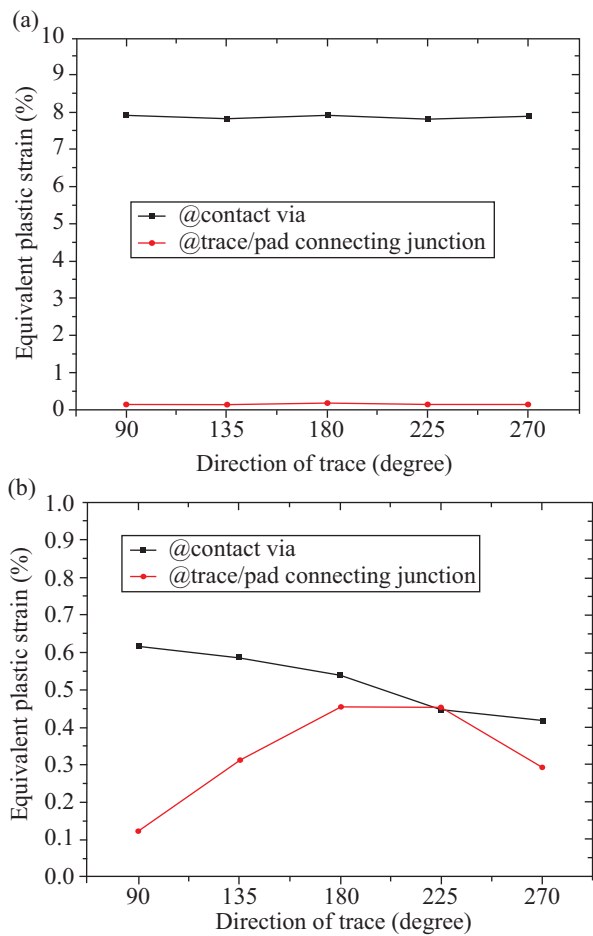

Fig. 17 Effect of trace direction (a) strain values of the first RDL; (b) strain values of the second RDL.

6.4 Effects of Curved Structure

As shown in Fig. 18, the U-shaped meandering line is designed as a stress-release structure for comparison with the straight metal line in the FE analysis. The curved portion does not affect the reliability of the first RDL. However, the U-shaped structure obviously reduces the strain values at the via of the second RDL, as shown in Fig. 19. The curved portion can absorb the expansion of the metal line and filler material, thus reducing the stress concentration occurring at the via. In addition, the trace/pad junction will be deformed significantly due to the curved structure, and the strain values at the junction will increase as the curved portion is introduced.
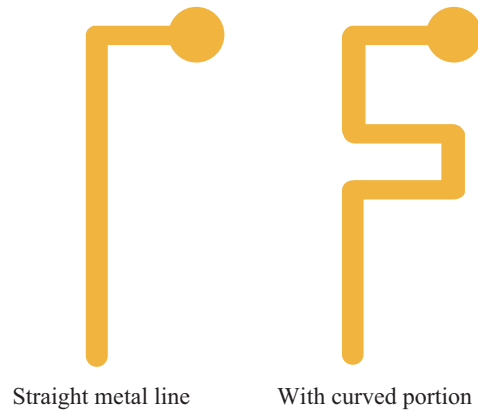

Straight metal line   With curved portion

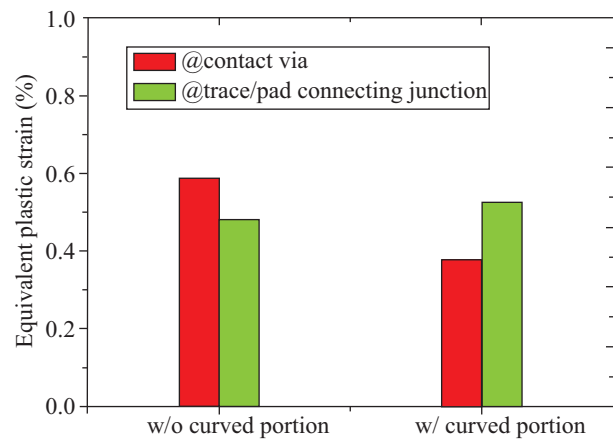Fig. 18 Breakdown drawing of designed redistribution lines for curved structure.

Fig. 19 Effect of curved structure at the second RDL.

6.5 Effects of Contact Via Location

In advanced electronic packaging, the I/Os from the IC are redistributed to the pads and connect with the PCB through solder joints. Conventionally, the layout of the solder joints depends on the function of the die and the corresponding PCB, such as in the NAND flash die application. It is hard to adjust the layout of the pad. However, the position of die pads can be modified easily via the semiconductor process. A RDL is also designed to study the effects of the distance from the copper via to the chip edge (D), as shown in Fig. 20. The results

show that the corresponding equivalent plastic strain increases as the contact via extends farther from the chip edge because the longer trace in the chip region will experience increased bending effect.
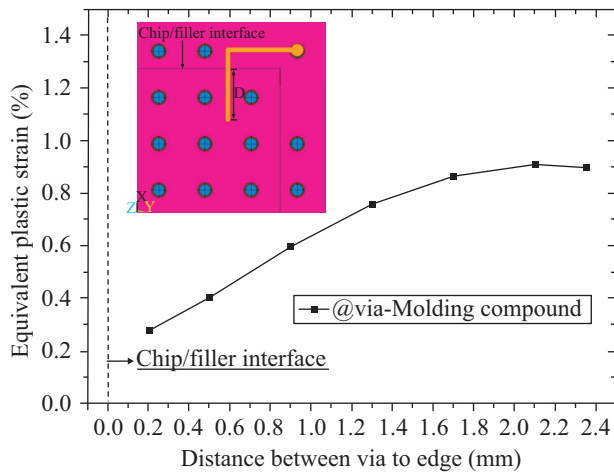

Fig. 20   Effect of contact via location.

6.6   Effects of Passivation Material

As shown in Fig. 17 (a) and (b), the equivalent plastic strain at the contact via of the first RDL is much higher than that of the second RDL.   To enhance the reliability of the contact vias in the proposed structure, the passivation material that surrounds the first RDL is replaced by polyimide.   The material properties of polyimide are shown in Table 3.   Figure 21 shows the equivalent plastic strain of the copper vias and indicates that the strain value drops significantly when polyimide is selected as the passivation material.   This is attributed to the fact that a stiff passivation material can prevent the deformation of the first RDL caused by out-of-plane movement.
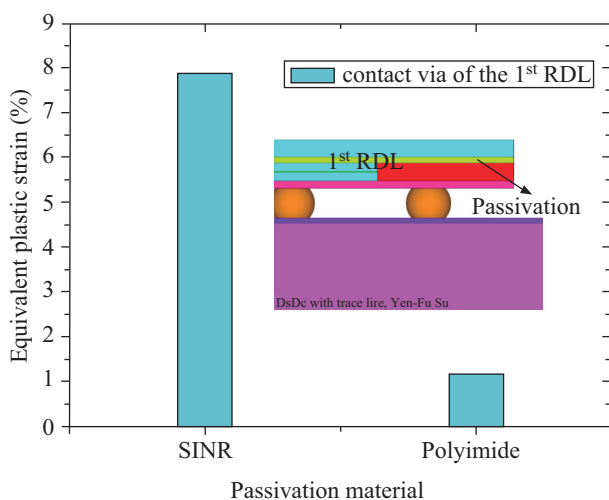

Fig. 21   Effect of passivation material.

7.   CONCLUSIONS

In this research, a double-chip stacking structure in an embedded fan-out WLP with double-sided interconnections is proposed.   The fine-pitched chip can be compatible with a coarse-pitched PCB to resolve the interconnection gap through RDLs.   To assess the reliability of the proposed design, a board-level FE model is established to investigate the thermo-mechanical behavior.   The major driving forces are CTE mismatches of the silicon carrier/molding compound and the package unit/PCB.   The lifetimes of solder joints and redistribution lines can be predicted via the Coffin-Manson relation and the Engelmaier model with mesh densities that have been validated, and both the reliability of the solder joints and the RDLs is more than 1,000 cycles.   Parametric analysis suggests that the application of a soft lamination material of suitable thickness can effectively release the stress on the solder joints.   Also, the selection of a carrier material whose CTE is close to that of the PCB can reduce the CTE mismatch.   Further, a trace/pad junction whose direction is parallel to the major direction of the CTE mismatch is recommended.   The curved portion can absorb the expansion of metal lines and filler material, thus reducing the stress concentration that occurs at the via.   Because the contact via is far from the chip edge, the longer trace would suffer more bending effect.   However, the strain values of the first RDL do not vary with the change in the trace layout.   To diminish the equivalent plastic strain occurring at the copper vias, a stiff passivation material can prevent the deformation of the first RDL caused by out-of-plane movement.   Accordingly, this research has proposed an overall reliability assessment through FE analysis to reduce time-to-market and fabrication costs of novel packaging structures.

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