

Evaluation of Defect Structures from *In Situ* Dielectric Breakdown of SiO₂-Based Gate Dielectric Layers

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For SiO₂-based gate dielectrics, the thickness of the dielectric layer approaches the diameter of the intrinsic ring structure of SiO₂. Intrinsic and extrinsic defects in the dielectric layer lead to reduced electron mobility along or leakage current across the gate channel. Leakage current across the gate dielectric indicates that the thin oxide layer fails to keep the gate capacitance. Such effects are commonly known as dielectric breakdown (BD) [1].

We present results of *in situ* TEM studies that were carried out to evaluate defect generation and subsequent dielectric breakdown of ultrathin SiO₂ dielectric layers in Co-silicide/poly-Si/SiO₂/Si field-effect transistor devices. Defect evolution under electrical stress provides information on the nanoscopic mechanisms of dielectric breakdown which, to date, remain unclear [2]. Time dependent dielectric breakdown (TDBD) of 3 nm SiO₂ dielectric layers was studied by *in situ* TEM using a double-tilt Nanofactory STM-TEM sample holder. A constant electrical bias was applied to the gate electrode and the resulting leakage current across the dielectric oxide layer was measured as a function of time during simultaneous TEM imaging of the atomic multilayer structure. Structural and chemical characterization of the device was done before, during, and after dielectric BD through HRTEM using a JEOL JEM 2500SE and an aberration corrected JEOL JEM 2100F/Cs that is equipped with a Gatan Quantum EELS Spectrometer.

HRTEM image acquisition during time-dependent leakage current measurements positively identified three stages of dielectric BD, i.e. wear-out, soft breakdown at +6.5 V and hard breakdown at +10.5 V [3]. Figure 1 shows conventional TEM micrographs of one device structure before and after dielectric breakdown induced during the STM-TEM experiment. Electrical stress-induced modifications of the gate electrode, the dielectric layer and the silicon substrate can be observed through changes in the diffraction contrast. Within the dielectric layer, local dielectric breakdown sites were identified through HRTEM and EELS observations of dielectric breakdown induced epitaxy correlated with locally reduced oxygen stoichiometry, respectively [3]. Furthermore, damaging to the substrate (wavy structure in Figure 1b) and Co migration from the gate electrode to the SiO₂ layer were observed (Figure 2). EELS spectrum imaging revealed oxygen diffusion from the SiO₂ layer into the substrate (Figure 2) due to a reduction-oxidation reaction at the SiO₂/Si interface that was activated by the applied electrical stress [3].

References:

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 [4] The authors acknowledge financial support through start-up funds from the University of California at Davis. Technical assistance by Ray Twesten and Paul Thomas (Gatan) during the EELS acquisition is greatly appreciated. Sample preparation by FIB sectioning was carried out at the National Center for Electron Microscopy (NCEM).

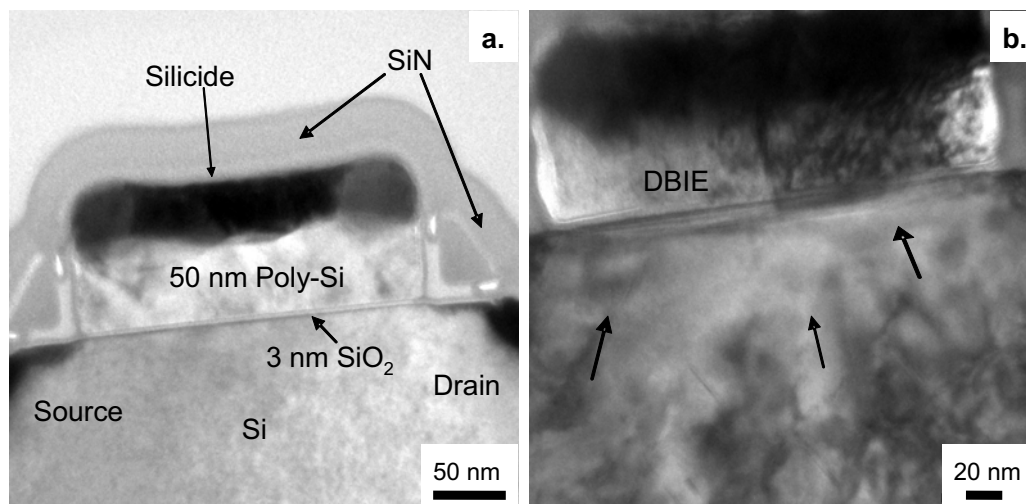


Figure 1. Co silicide/Poly-Si/SiO₂/Si device structure before (a) and after (b) dielectric BD [3].

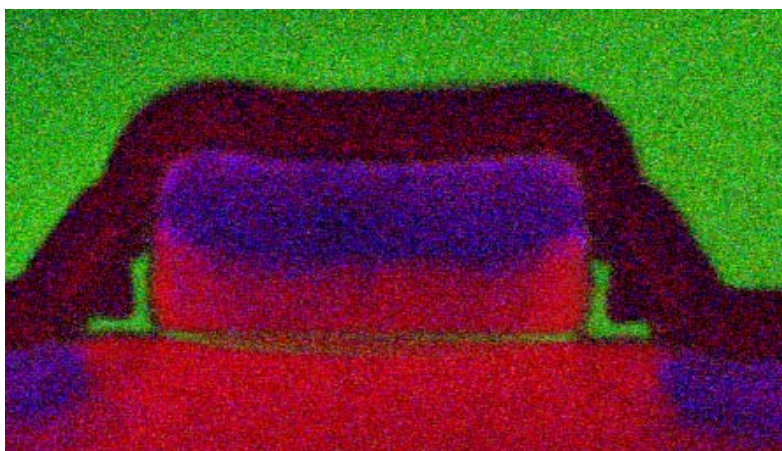


Figure 2. Elemental distribution map from integrated EELS intensities for the Si L_{2,3} (red), O K (green) and Co L_{2,3} (blue) absorption edges.