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Novel Field Effect Transistor Fabrication Based on Non-Graphene 2D Materials

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ABSTRACT

In this paper, field effect transistors (FET) based on different kinds of non-graphene materials are introduced, which are MoS_2, WSe_2 and black phosphorus (BP). Those devices have their unique features in fabrication process compared with conventional FETs. Among them, MoS_2 FET shows better electrical characteristics by applying a SiO_2 protective layer; WSe_2 FET is fabricated based on a new low pressure chemical vapor deposition (LPCVD) method; BP FET acquires high on/off ratio and high hole mobility by using a simple dry transfer method. Those novel non-graphene materials inspire new design and fabrication process of basic logic device.

INTRODUCTION

Field effect transistor (FET) as the basic logic device plays an important role in information age. Novel two-dimensional (2D) materials show great promise for the next generation low-dimensional FET. However, the FET based on a well-known 2D material, graphene, shows bad on-off radio due to its zero bandgap property. Therefore, beyond graphene, new kinds of non-graphene materials with reasonable bandgap, such as MoS_2, WSe_2 and black phosphorus (BP), have attracted wide research attention. Unique FET fabrication process was designed for these non-graphene 2D materials to obtain FET with higher mobility and on-off radio. Here, three works about novel field effect transistor fabrication based on non-graphene 2D materials are presented and discussed.

MoS_2 FETs with a SiO_2 protective layer

A. Introduction

Top-gate MoS_2 FETs with SiO_2 protective layer were fabricated to avoid the monolayer MoS_2 from the influence of charged impurities and interface states by designing unique optical lithography process. As a result, the contact property between the MoS_2 and the electrodes were improved and both the carrier mobility and the source-drain current were enhanced. Comparing with MoS_2 FETs without a SiO_2 protective layer, the SiO_2 protective layer was found to enhance the transfer and output characteristics of MoS_2 FETs. This work applies a practical method to enhance the MoS_2 FETs performance in the low-dimensional FET fabrication process.

B. Monolayer MoS_2 characterization and device fabrication

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The details of monolayer MoS_2 growth on SiO_2/Si substrate by CVD method were referred in Ref.1. [1] The AFM image in Figure 1 (a) shows the uniformity of the MoS_2 material with a thickness of ~ 0.71 nm， which accords with the thickness of monolayer MoS_2 well. The red and blue lines in the Figure 1 (b) present the Raman spectrum of MoS_2 material before and after 10 s buffer oxide etching (BOE) process, which are nearly overlapped and indicate that the BOE liquid did not etch the MoS_2 layer. The difference of the two peak in the Ramon spectrum is 19.5 cm^{-1}, which demonstrates the MoS_2 layer is a monolayer.

Two different MoS_2 FETs structures with and without 10 nm SiO_2 protective layer were shown in Figure 1 (c) and (d), respectively. Figure 2 shows the fabrication process of the MoS_2 FETs structure with a SiO_2 protective layer. 10 nm SiO_2 layer was deposited on the MoS_2 surface by ALD to protect the MoS_2 layer from being exposed to the photoresist and other object. By the first lithography step, extra SiO_2 protective layer was etched using 10s BOE process and 25 nm Ti electrodes were deposited on the MoS_2 layer. After the second lithography, the extra SiO_2 and MoS_2 layer were etched by the second BOE process and O_2 plasma, respectively. Finally, the high-k HfO_2 dielectric and Al top gate electrodes were made by conventional fabrication process and MoS_2 FETs structures with SiO_2 protective layer were achieved.

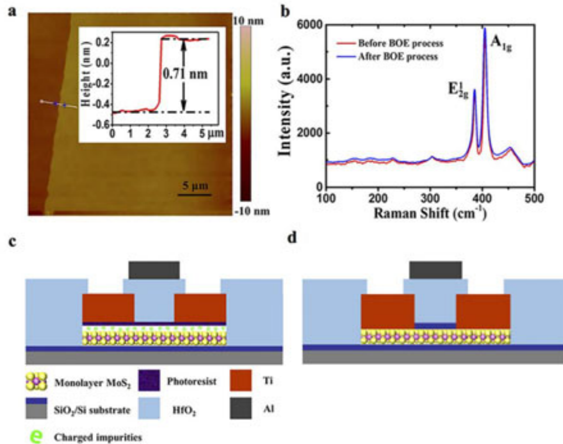

Figure 1. (a) AFM image of the MoS_2 grown on SiO_2/Si substrate by CVD. (b) The Raman spectroscopy measurements on the monolayer MoS_2 material. (c) Schematic perspective view of CVD-grown monolayer MoS_2 FETs without a SiO_2 protective layer. (d) MoS_2 FETs with a SiO_2 protective layer.

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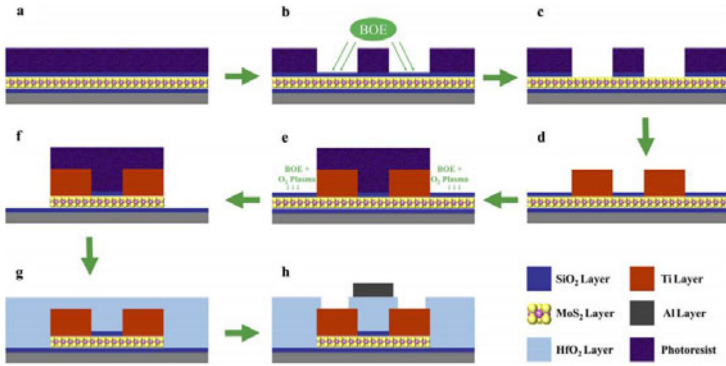

Figure 2. The process of the SiO_2 protective layer technology. (a) Depositing 10nm SiO_2 and coating photoresist on the prepared monolayer MoS_2 material. (b) Patterning the metal electrodes and etched SiO_2 by BOE liquid. (c) The SiO_2 layer was etched. (d) Depositing 25nm Ti metal by lift-off. (e) Etching SiO_2 by BOE liquid and etching MoS_2 material by O_2 plasma. (f) The MoS_2 was etched. (g) Depositing top-gate dielectric 30nm HfO_2 by ALD. (h) Etching the HfO_2 to expose the source/drain electrodes and depositing top-gate electrode Al.

C. Electrical characterization of MoS_2 FETs with a SiO_2 protective layer

Figure 3 shows the measured electronic characteristics of a top-gate monolayer MoS_2 FET with a SiO_2 protective layer, whose channel length and width are both 4 μm. Figure 3 (a) shows the transfer characteristics (red line) of the FET at V_{ds} = 1 V in which the drain-source current (I_{ds}) varies as a function of top-gate voltage (V_{gs}). At V_{ds} = 1 V, the current on/off radio is ~ 5×10^6 and the FET mobility (μ) calculated by the equation:

$$\mu = \frac{dI_{ds}}{dV_{gs}} \cdot \frac{L}{W} \cdot \frac{1}{C_g \cdot V_{ds}}$$

The FET mobility is ~ 42.3 $cm^2/V{\cdot}S$, which has increased ~ 20 times compared to the previous MoS_2 FET fabricated without the SiO_2 protective layer.[2] Figure 4 (b) shows the transfer characteristics at different V_{ds} ranging from 0.025 V to 1 V which exhibits a typical n-type behavior. The output curves shown in the Figure 3 (c) present the saturation properties of the monolayer MoS_2 FET, in which the ohmic contact characteristics can be observed at lower $V_{ds.}$ Compared with the non-ohmic contact in the MoS_2 FET without the SiO_2 protective layer, it can be obviously claimed that the performance of the MoS_2 FET can be largely improved by applying a SiO_2 protective layer. [2]

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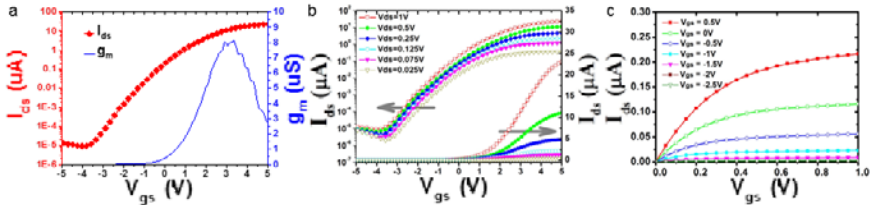

Figure 3. Electrical characterization of MoS_2 FETs with a SiO_2 protective layer. (a) Red curve shows the transfer characteristics of a top-gate CVD grown monolayer MoS_2 FET with SiO_2 protective layer. The blue curve shows the transconductance of the FET. (b) Transfer characteristics of the FET for V_{ds} ranging from 0.025V to 1V. (c) Output characteristics of the FET for the V_{gs} ranging from -2.5V to 0.5V.

WSe_2 FETs based on LPCVD process

A. Introduction

In this work, large-scale growth of high-quality WSe_2 atomic layers directly on SiO_2/Si substrates using a low pressure chemical vapor deposition (LPCVD) method was reported. The influence of growth temperature, carrier gas flow rate and tube pressure was investigated, which affects the sizes, shapes and the thickness of as-grown WSe_2 flakes. By applying a pre-annealing step, the quality of WSe_2 flakes improve a lot which show the lateral size up to 30 μm and monolayer thin film area of 0.25 mm^2. After that, raman spectrum, microphotoluminescence and auger electron spectroscopy (AES) were performed to characterize the as-grown WSe_2 flakes. Finally, p-type WSe_2 field-effect transistors were fabricated using the WSe_2 flakes which exhibit excellent electrical properties with carrier mobility of $\sim 64\ cm^2 \cdot V^{-1} \cdot s^{-1}$ and current on/off ratio over 10^5. This work opens a new way for the customized low-dimensional non-graphene FET fabrication.

B. Larger scale single crystal WSe_2 growth by LPCVD process

The LPCVD process was performed in a homemade tube furnace with a vacuum pump and pressure meter. After a specific annealing process (see Ref.3 for details), WSe_2 powder (0.2 g) was placed in a quartz boat at the center of a quartz tube, and the clean SiO_2/Si substrates were used as the growth substrate at the downstream with variable temperature. High-purity Argon gas with a designed flow rate was continuously supplied as the carrier gas and the pressure in the tube was pumped down to 10 Pa during the whole growth process. The tube furnace was heated up to 1060 °C in 30 mins and maintained 30 mins for growth. Finally, the whole system was naturally cooled down to ambient temperature.

The as-grown WSe_2 flakes was observed by optical microscope (OM) shown in Figure 4 to Figure 6. Figure 4 shows the influence of temperature on WSe_2 growth, demonstrating larger area flakes begin to appear and merge together with temperature decreasing. However, when the temperature became lower, WSe_2 flakes disappeared and WSe_2 nanoflowers began to form. Figure 5 shows the WSe_2 growth at different tube pressures, indicating suitable lower tube pressure can increase the WSe_2 film size. Figure 6 shows the optical images of the as-grown

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WSe_2 flakes under an Ar flow rate of 200 SCCM and the layer number and the domain size of WSe_2 are increased with the increasing of the gas flow rate. Besides, Raman spectrum, microphotoluminescence and auger electron spectroscopy (AES) were performed to characterize the as-grown WSe_2 flakes in Figure 7, which confirm the monolayer, uniformity and chemical composition of the WSe_2 flakes.

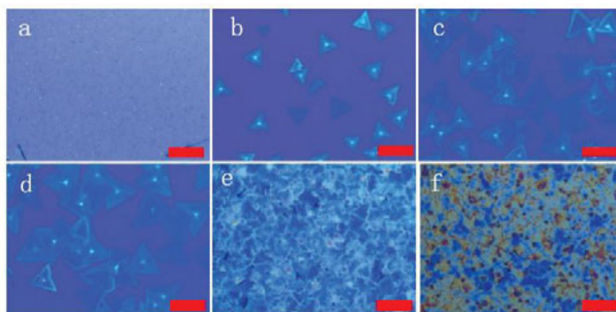

Figure 4. WSe_2 growth with temperatures varying from 850˚C to 700˚C. Optical microscope images of WSe_2 samples grown at different temperatures under a designed flow rate and vacuum degree (100 SCCM, 200 Pa) for 30 min: (a) 850˚C, WSe_2 particles; (b) 800˚C, WSe_2 flakes; (c) 780˚C, larger WSe_2 flakes; (d) 760˚C, larger WSe_2 flakes; (e) 750˚C, WSe_2 film and (f) 700˚C, WSe_2 nanoflowers. All the scale bars are 20 µm.

Figure 5. Optical images of WSe_2 with different growth pressures: (a) 280 Pa, (b) 180 Pa and (c) 70 Pa. All the scale bars are 20 µm and the temperature used for the pressure dependency study is 765˚C.

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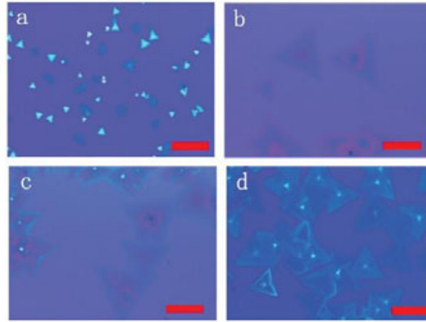

Figure 6. Optical microscope images of large WSe_2 samples grown under an argon flow rate of 200 SCCM for 30 min. From (a) to (d), the temperature decreases from 850˚C to 750˚C. All the scale bars are 20 μm.

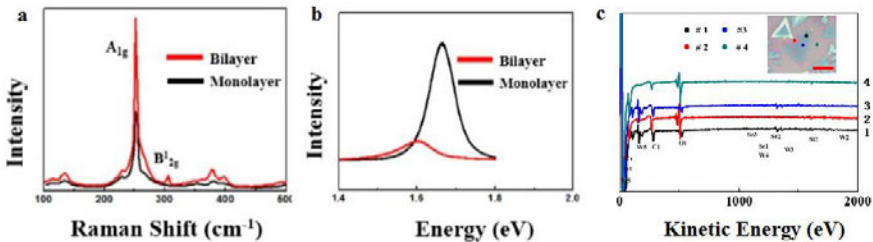

Figure 7. (a) Raman characterization and (b) photoluminescence characterization of monolayer and bilayer WSe_2. (c) AES spectra of the as-grown WSe_2 flakes under an argon flown rate of 200 SCCM at 765 ˚C for 30 min.

C. Electrical characterization of the monolayer back-gated WSe_2 FET

The as-grown WSe_2 flakes were subsequently used to fabricate back-gated FETs by electronic beam lithography. 5 nm Ti and 25 nm Au were evaporated on the WSe_2 flakes to make the source and drain. Figure 8 shows the transfer curves and output curves of the WSe_2 FETs. The typical I_{SD}-V_{GS} curve in Figure 8 (a) indicates a p-type behavior while the linearity of I_{DS}–V_{DS} curves demonstrates ohmic contacts were formed at the source and drain electrodes. The charge mobility and on/off current ratios of the FETs were ~ 64 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 10^5 respectively, which are comparable to the reported results based on exfoliated WSe_2. [3]

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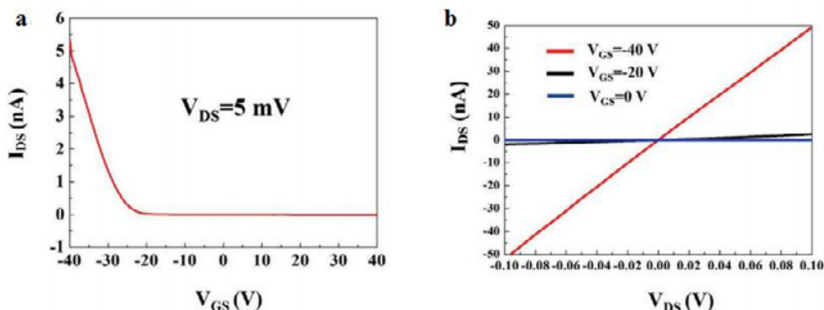

Figure 8. Electrical characterization of the monolayer WSe_2 based back-gated FET device. (a) I_{DS}-V_{GS} plots of back-gated FET at V_{DS} = 5 mV. (b) I_{DS}-V_{DS} output characteristics at V_{GS} = 0, -20V and -40 V.

BP FET based on a simple dry transfer method

A. Introduction

An as-prepared BP FET was fabricated using a simple dry transfer method to minimize polymer residues and avoid the liquid immersion process compared with conventional material transfer process. As a result, BP with little degradation was achieved while the BP FET exhibited excellent electrical properties with a relatively high on/off ratio of 10^4 and a high hole mobility exceeding 380 $cm^2/(V \cdot s)$. Besides, due to the degradation and doping effect, BP shows a time-dependent electrical property indicating the declining and recovering process. Finally, it was demonstrated that the degradation and large-scale hysteresis of BP FET could be modified by covering a thin Al_2O_3 layer.

B. BP characterization and device fabrication

The details of BP using a simple dry transfer method were referred in Ref.4 [4]. The AFM image in Figure 9 (a) shows the uniformity of the dry-transferred BP with a thickness of only 5 nm, demonstrating the transfer technique performed well. However, the three obvious peaks (A_{1g}, B_{2g}, and A_{2g}) of the Raman spectrum in Figure 9 (b) indicate that the dry transferred BP is not monolayer. [6]

The all-dry transfer process for fabricating BP FET is shown in Figure 10. Firstly, thin-layer BP was exfoliated onto a transparent poly (vinyl chloride) (PVC) film and adhered the film to the micromanipulation platform. After that, the few-layer BP was transferred onto the stripe-shaped electrodes on the Si/SiO_2 substrate by pressing the PVC film down. Finally, lift up the film and the target BP was left on the electrodes to achieve a BP FET with bottom electrodes. It is worth noting that the air exposure time should be limited to 10 min during the fabrication and an annealing process is necessary to improve the contact between electrodes and BP, in which the sample is heated at 200 ℃ in an argon environment for 20 min.

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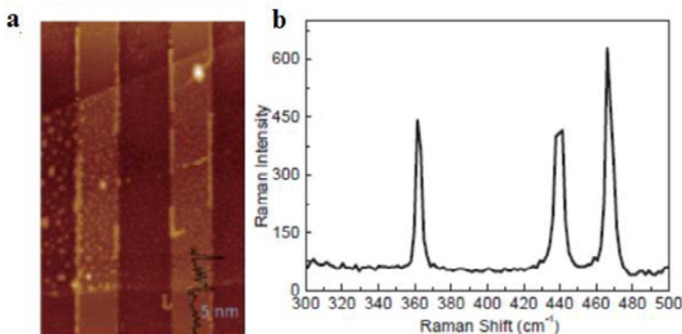

Figure 9. (a) AFM image of the BP using a simple dry transfer method. (b) The Raman spectroscopy measurements on the BP material.

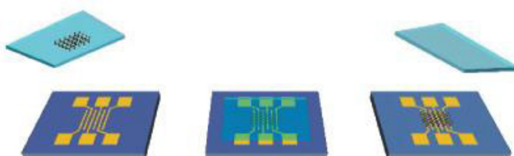

Figure 10. The all-dry transfer process for fabricating BP FET.

C. Electrical characterization of BP FET

The electrical property of BP FET was measured in ambient atmosphere shown in Figure. 11. The on-state current reached up at 0.01 V drain bias and the on/off ratio exceeded 10^4. The hole mobility was calculated up to 380 $cm^2/(V \cdot s)$, which is comparable to those in other related literatures where BP FET was fabricated in a glove box or measured in vacuum. [5] Figure. 11 (b) shows the output characteristic of BP FETs[6]. For a negative back gate voltage, the current tends to saturate at a high drain bias because of pinch-off. However, the drain current exhibited Schottky behavior when the back gate voltage was more than 0 V, which was demonstrated in other work as well. [5]

Figure 12 (a) shows the transfer curve measured under different times, indicating that the electrical conduction of BP was quickly changed from declining to recovering. After depositing a Al_2O_3 protection layer, the transfer curves of BP FET with initial state and 150 min exposure to ambient atmosphere were shown in Figure 12 (b) and (c). The limited changes in the two curves demonstrate the excellent protective function of Al_2O_3 layer. This research has great significance to the fundamental researches and applications of BP. [4]

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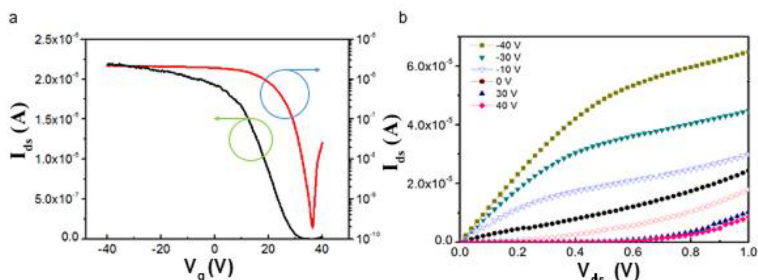

Figure 11. (a) The transfer curve at 0.01 V drain bias. The black and red curves are plotted in linear and logarithmic scales, respectively. (b) The output characteristic of BP FETs under different gate voltages.

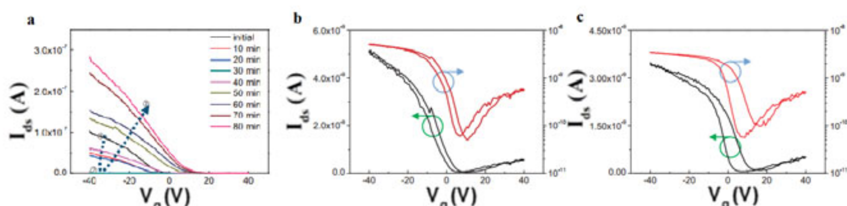

Figure 12. (a) Time-dependent electrical property of BP FET. The dashed arrow shows the change in electrical property. (b) Transfer curve of BP FET with 30 nm Al_2O_3 as protection layer. (c) Transfer curve after 150 min exposure to ambient atmosphere of the same FET.

CONCLUSIONS

Three works related to non-graphene 2D materials FETs are presented in this paper. The inserted SiO_2 protective layer enhances the carrier mobility and the source-drain current of MoS_2 FETs. And larger scale single crystal WSe_2 growth by LPCVD process shows the potential to fabricate wafer-scale logic circuits. Moreover, BP FET based on a simple dry transfer method provides a process to improve the performance of the device based on unstable materials. These novel non-graphene based FETs processes inspire new design of basic logic device and their application in electronic systems.

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