DETECTOR CONTROLLERS FOR THE GALILEO TELESCOPE: A PROGRESS REPORT

G. Bonanno, P. Bruno, R. Cosentino,

Osservatorio Astrofisico di Catania

F. Bortoletto, M. D'Alessandro, D. Fantinel,

Osservatorio Astronomico di Padova

A. Balestra and P. Marcucci

Osservatorio Astronomico di Trieste

1. INTRODUCTION

The GALILEO telescope requires a flexible detector controller that allows one to drive single and mosaic CCDs in different modes of operation. The CCD controller can be divided into two main parts: the preamplifier, located close to the cryostat and the other modules, the Sequencer, the Bias generator, the Clock driver, the Preamplifier and the Correlated double sampler, located into a rack and connected together via a CCDC-BUS.

2. MAIN FEATURES OF THE CCD CAMERA

For the TNG focal planes, we have chosen the Loral three-side buttable CCDs (2048 X 2048 pixels, 15 μm pixel size). Each CCD can be read on two outputs. The controller is able to drive 2 x 2 mosaics and the readout time is compatible with a single chip system. The image is at once reformatted to simulate a single sensor having the full mosaic size.

3. CCD SEQUENCER

The functions supported by the CCD SEQUENCER are: a clock waveform generation for CCD and signal processor; setting the time and monitoring of CCD bias levels (clocks and analog levels); handling of the local data-buffer and telemetry; file making up; commands reception and handling and shutter and temperature-controller handling.

Possible CCD readout modes are: full frame, only a set of predefined boxes with fast skip of unwanted pixels, with binning, drift scan mode. In drift scan mode, synchronization can be provided externally. The heart of the CCD sequencer is a standard TRAM module (DTM560) containing a couple of high speed processors: a 16 bit T222 INMOS transputer and a 24-bit 56001 MOTOROLA DSP. The Transputer and DSP communicate data and application SW through a set of shared memory locations. Thanks to the simple reconfigurable networking scheme embedded on the transputer, fast communication of data and commands can be easily

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implemented with little extra hardware.

Sequences can be generated in two DSP ports: PORT A that allows 16 independent sequencer status lines and PORT B that allows 12 independent sequencer status lines. The status and the delay loop are derived from a given table. An eight-bit counter is programmed with the upper eight bits of the DSP-24 bit word while the lower 16 bits are used as programmable sequencer lines. The counter holds the DSP in WAIT state until the counter rollover; each tick corresponds to 100 ns (the DSP clock is 20 MHz), so a maximum delay of 25.6 μs can be programmed. Longer delays, when needed, can be obtained by conventional SW loops.

4. PROGRAMMABLE BIAS GENERATOR

The board that generates the Bias levels has the following features; 32 buffered output voltages providing at least 10 mA (These are programmable through 8-bit D/A converters with serial loading (DAC 8800 PMI); 16/1 multiplexers with selection latch allowing the choice between 32 analog signals and a 12-bit ADC (ADC 674A Burr Brown) with 15 μs conversion time used for telemetry; DSP data-bus used for ADC programming and telemetry.

The board is a single euro card and is realized by using "Surface Mount Device" technology. The DSP 24-bit data bus is used for programming the DACs and for receiving data from the telemetry section. The addressing and the control logic for D/A programming and multiplexers driving are also provided. The DAC output is unable to drive other devices directly, so we utilize operational amplifiers (OP490) to buffer the output.

5. CLOCK DRIVER

The clock driver board performs the level translation and buffering of signals coming from the sequencer. Low and high levels are programmable and their values are monitored by telemetry. The circuit employed for the voltage level generation is the same as the bias generator board. Fast switches (AD7512), in conjunction with a fast buffer (LM6321) are used to drive the CCD. To introduce fixed rise and fall times a resistor-capacitor circuit is used.

6. CORRELATED DOUBLE SAMPLER

The correlated double sampler (CDS) performs the subtraction between the baseline signal and the CCD output signal. Two operating modes are allowed: a. The integrator performs either the integration, for a fixed amount of time, and the difference of both signals. The difference is converted by the ADC, b. Both signals are integrated and converted, the binary difference is performed by transputer. The ADC module, that consists in a size two TRAM format board, is plugged in the CDS board. This solution allows the replacement of different ADCs, with different resolution and conversion times.