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Strain Quantification Analysis of Epitaxial SiGe on SOI by Nanobeam Diffraction (NBD)

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Strain engineering technology is now routinely integrated in the wafer fabrication process to increase the carrier mobility and improve the device performance. Measuring and controlling the strain in nanoscaled materials is a critical for developing the state-of-art semiconductor devices [1-2]. High-performance strain-engineered ETSOI devices have been reported, such as strained SOI (SSDOI) for NFET and SiGeon-insulator (SGOI) for PFET [3-4]. Characterization of strain within channel area is very important to understand integration and device performance. In this work, we investigate the strain distribution in two samples. One is 27 nm SiGe epitaxially grown on 7 nm ETSOI substrate. The other is 21nm SiGe epitaxially grown on 9nm ETSOI substrate, followed by thermal anneal to drive Ge into the underlying ETSOI layer to form a uniform SiGe layer. Fig.1 shows the schematic thermal mixing flow to form SiGe channel ETSOI. The strain in the original epi SiGe layer is transferred into SOI region and can be maintained after the thermal anneal process, which could be beneficial for device fabrication. Line scan of diffraction patterns perpendicular to the SiGe/ETSOI film stack were acquired and the reference diffraction pattern of unstrained Silicon was acquired from the bulk Si substrate below the buried oxide (BOX). The strain is then calculated by comparing the diffractions patterns acquired in the region of interest (e.g., SiGe) with a pattern acquired in a reference unstrained Si substrate Since the software uses Si lattice constant as reference, the lattice deformation profile is actually generated.

Fig. 2 shows the high-resolution dark field STEM image of the as-grown SiGe layer as well as the one with thermal anneal. No crystalline defects were observed on either sample, indicating good film quality.

(100) wafer was used in this work and electron diffraction patterns were taken at <110> zone axis. The (022) and (002) diffraction reflections have been selected to measure the lattice deformation in the horizontal (in-plane) direction and in the vertical (out-plane) direction, respectively. Line profiles of lattice deformation for two directions are shown in Fig.3. Out-plane deformation can be clearly seen in SiGe layer compared to underlying ETSOI layer (Fig.3(a)). No obvious in-plane deformation was observed in either sample, indicating the SiGe layer is fully strained and no obvious relaxation occurs within the measurement accuracy (~0.1%). Same batch of wafers were also characterized by µXRD to obtain Ge content in this two specimens. With known Ge concentration, the lattice constant for fully-relaxed SiGe can be calculated. The in-plane strain in both SiGe film can be calculated using relaxed SiGe as reference. The compressive in-plane strain for as-grown SiGe and the annealed SiGe is ~ -0.7% and -0.6%, respectively. The strain values are consistent with our XRD measurement data. After thermal anneal, the epi SiGe/ETSOI turns into one uniform SiGe layer and is fully strained. The line profile of lattice deformation indicates the compressive strain is distributed uniformly within this single SiGe layer. SiGe FinFET device fabrication is still ongoing. NBD strain analysis including line profile and strain mapping will be performed on device specimens.

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In summary, the NBD method has been demonstrated that it can provide the high spatial resolution and high strain sensitivity for strain analysis in semiconductor materials. Thermal mixing of epi SiGe and ETSOI can form a uniform SiGe layer without strain relaxation. The fully strained SiGe on insulator (SGOI) can be used for next generation SiGe FinFET device or SiGe channel ETSOI device.

Reference

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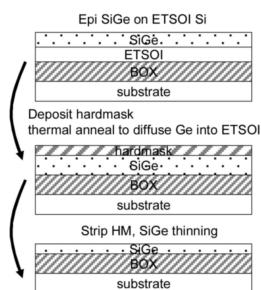
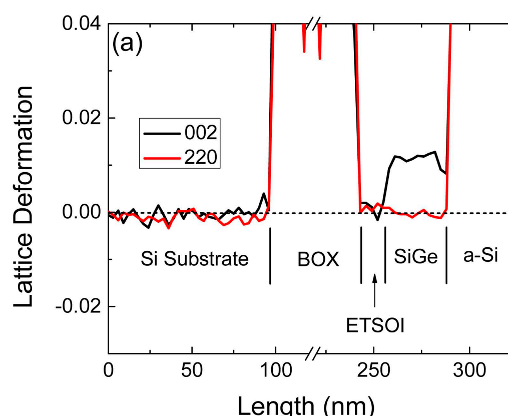


Fig.1 Schematic process flow (thermal mixing) to form SiGe channel ET SOI.



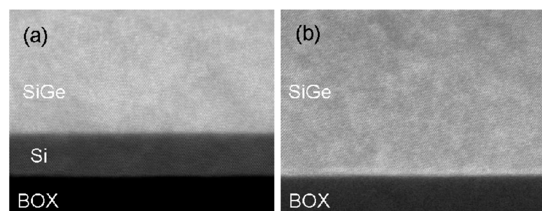


Fig.2 High-resolution dark field STEM image of (a) as-grwon SiGe on ETSOI and (b)SiGe on ETSOI with thermal anneal.

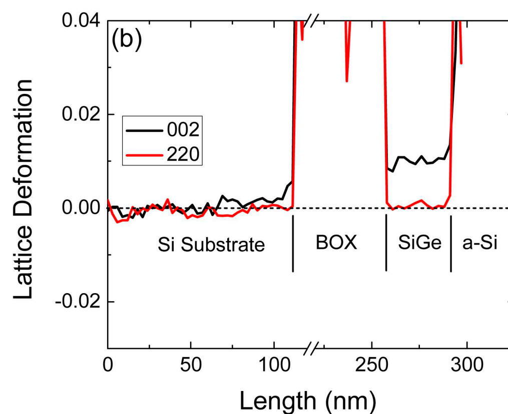


Fig.3. Lattice deformation line profile accquired by NBD. (a) 27 nm epi SiGe (20% Ge by XRD) on 7 nm ETSOI substrate, and (b) 21 nm epi SiGe on 9 nm ETSOI with thermal anneal (13% Ge by XRD).

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