FABRICATION AND CHARACTERIZATION OF GaN JUNCTIONFIELD EFFECT TRANSISTORS

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ABSTRACT

Junction field effect transistors (JFET) were fabricated on a GaN epitaxial structure grown by metal organic chemical vapor deposition. The DC and microwave characteristics, as well as the high temperature performance of the devices were studied. These devices exhibited excellent pinch-off and a breakdown voltage that agreed with theoretical predictions. An extrinsic transconductance (g_m) of 48 mS/mm was obtained with a maximum drain current (I_D) of 270 mA/mm. The microwave measurement showed an f_T of 6 GHz and an f_{max} of 12 GHz. Both the I_D and the g_m were found to decrease with increasing temperature, possibly due to lower electron mobility at elevated temperatures. These JFETs exhibited a significant current reduction after a high drain bias was applied, which was attributed to a partially depleted channel caused by trapped electrons in the semi-insulating GaN buffer layer.

INTRODUCTION

Wide bandgap GaN and its related materials have great potential for high power and high temperature microwave electronic device applications owing to their low intrinsic carrier concentration, high breakdown field, high saturation velocity, and excellent chemical stability [1-3]. A significant amount of effort has been devoted to the development of various GaN-based field effect transistors (FETs) [4-8], which has led to the demonstration of high performance GaN/AlGaN MODFETs [9-12]. Compared to MESFETs and MODFETs, JFETs provide a higher gate voltage swing and a lower reverse gate leakage current due to a higher built-in potential of the p-n junction gate than the Schottky gate used in MESFETs and MODFETs. This is especially important for high temperature operation. In addition, the junction gate is metallurgically more stable and environmentally more robust than a Schottky gate since it is effectively buried beneath the surface and is subjected to high temperature during crystal growth. Therefore, JFETs are expected to withstand higher temperature operation than MESFETs and MODFETs. In this paper, we report the fabrication and characterization of epitaxially grown GaN JFETs.

MATERIAL AND FABRICATION

The epitaxial structure of GaN JFETs was grown by metal organic chemical vapor deposition (MOCVD) on a C-plane sapphire substrate. The layer structure consisted of a 4.2 µm semi-insulating GaN buffer layer, a 950 Å Si-doped n-GaN channel, a 60Å undoped GaN, and a 500 Å Mg-doped p-GaN. The sample was annealed at 850 °C for 15

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sec in N_2 to activate the Mg dopant. Hall measurements showed a free carrier concentration of $1.3x10^{18}$, $2.4x10^{18}$, and $6.1x10^{14}$ cm^{-3} in the p-GaN, n-GaN, and SI-GaN, respectively. The electron mobility in the n-GaN active layer was 270 cm^2/V-sec. The fabrication process began with a mesa isolation etch in an inductively coupled $BCl_3/Cl_2/Ar$ plasma. Next, a gate metal of Ni/Au/Ni was e-beam evaporated on top of the mesa and used as the mask for the self-aligned source-drain etch in a $BCl_3/Cl_2/Ar$ ICP discharge. The device was completed with Ti/Al source and drain ohmic contact metallization. Post-metallization annealing was not performed. A transmission line method (TLM) measurement showed an as-deposited source and drain ohmic contact resistance of 4.2 Ω-mm, a specific contact resistance of $5x10^{-5}$ Ω-cm^2, and a sheet resistance of 4700 Ω/square, respectively. These values were relatively large, possibly due to plasma induced damage and an overetched source and drain region.

RESULTS AND DISCUSSION

Table I summarizes the DC and microwave result of a 0.8 µm X 50 µm GaN JFET with a source-drain spacing of 3 µm. A maximum I_D of 270 mA/mm and a maximum g_m of 48 mS/mm were measured at V_G=1 V. A R_S of 8.5 Ω-mm and a R_D of 13 Ω-mm were obtained using the end resistance measurement technique. From the above result, an intrinsic transconductance (g_{m0}) of 81 mS/mm was calculated. The channel was completely pinched off at a threshold voltage of V_G=-8 V, with an I_D=210 µA/mm at V_D=15 V. A gate-drain diode reverse breakdown voltage of 56 V was achieved, which corresponded to a breakdown field of $2.5x10^6$ V/cm. The fact that the breakdown field approached the theoretical predicted breakdown field of GaN indicated that the relatively small breakdown voltage of the JFET as compared to the reported GaN MESFETs and MODFETs [4,12] was primarily due to the high doping concentration in the n-GaN. The gate leakage current of our JFETs was large as compared to GaN MODFETs [13,14], possibly due to the plasma induced damage to the junction [15, 16]. The forward turn-on voltage of the gate diode was ~ 1 V using a 1 mA/mm current criterion. This value is only 30% of the bandgap energy of GaN. Pernot, *et. al.* have also reported a low turn-on voltage of 1.2 V on GaN p-n diodes [17]. The cause of this low turn-on is not known at present but may result from defect levels in the GaN.

maximum drain current (I_D)	270 mA/mm
threshold gate voltage (V_T)	-8 V
knee voltage (V_{knee})	8 V
gate-drain diode breakdown voltage	56 V
gate turn-on voltage	~ 1 V
extrinsic transconductance (g_m)	48 ms/mm
parasitic source resistance (R_S)	8.5 Ω-mm
parasitic drain resistance (R_D)	13 Ω-mm
cut-off frequency (f_T)	6 GHz
maximum frequency (f_{max})	12 GHz

Table I: DC and microwave characteristics of a 0.8 µm X 50 µm GaN JFET.

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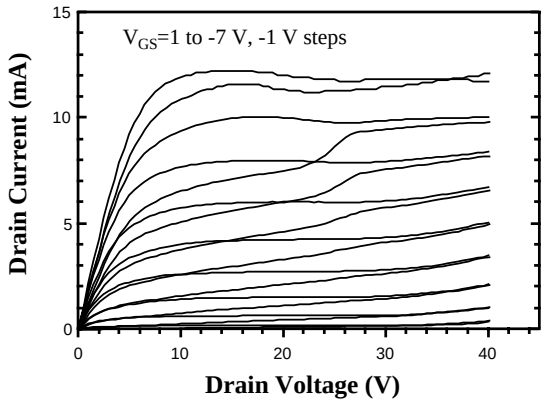

***Figure 1**: I_D-V_D characteristic showing the drain current collapse at V_D< 25 V due to a partially depleted channel by electrons trapped in the SI-GaN. The solid curves were measured individually with 5 min of illumination to release trapped electrons in the SI-GaN. The dashed ones were measured in rapid recession.*

Similar to what Binari and co-workers have reported on GaN MESFETs [4], a significant reduction in I_D occurred in our JFETs after they were subjected to a high V_D. Figure 1 shows two sets of I_D-V_D curves measured up to V_D=40V under white-light illumination. The solid curves were measured individually with 5 minutes of illumination before each curve was taken while the dashed curves were measured in rapid succession. The upper dashed trace (V_G=1 V) is nearly identical to the upper solid trace since they were both subjected to a long illumination. The subsequent dashed curves exhibited a large decrease in I_D at V_D<25 V. This current collapse effect was not obvious unless V_D was increased above 20V. The reduction in I_D was caused by high-field injection and subsequent trapping of electrons in the SI-GaN, which depleted part of the active channel from the backside. We have demonstrated that these trapped electrons were located at the drain side of the channel where the electrical field was the highest [18]. At V_D<5 V, the transistor was below saturation and the current was limited by R_S, R_D, and the channel resistance, R_{CH}. Since the channel was partially depleted by the trapped electrons, a lower channel conductance was obtained for the dashed I_D-V_D curves as compared to the solid ones in Figure 1. Above the knee voltage, it was assumed that the channel consisted of a velocity-saturated section in parallel with a space-charge region caused by trapped electrons in the GaN buffer. The latter was evidenced by the nearly constant output conductance between the knee voltage and V_D=25 V. The rapid increase in I_D of the collapsed curves at V_D~25V may indicate a local breakdown of the space charge region. Therefore, regardless of illumination, I_D at V_D>25V was limited by an undepleted, velocity-saturated region on the drain side of the space charge layer.

The microwave performance of the JFETs was characterized using an HP 8510 network analyzer. A unity current-gain cutoff frequency (f_T) of 6 GHz and a maximum frequency (f_{max}) of 12 GHz were obtained at V_D=15 V and V_G=0 V from the small-signal S-parameters. These values were comparable to the reported f_T and f_{max} on GaN MESFETs and GaN/AlGaN MODFETs with a similar gate length [19, 20]. The intrinsic f_T of our JFETs would be higher by taking into account the large source and drain resistance.

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Following the derivation made by Tasker and Hughes [21], we were able to calculate f_{T0} of the JFETs by de-embedding the effect of the parasitic R_S and R_D from measured f_T. From [21], the extrinsic cut-off frequency

$$f_T = \frac{g_{m0}/2\pi}{[C_{GS}+C_{GD}]\cdot[1+(R_S+R_D)/R_{DS}]+C_{GD}\cdot g_{m0}\cdot(R_S+R_D)}$$

where C_{GS}, C_{GD}, and R_{DS} are the gate-source, gate-drain capacitance, and output resistance, respectively. Rearranging this equation, the intrinsic cut-off frequency

$$f_{T0} \equiv \frac{g_{m0}}{2\pi(C_{GS}+C_{GD})} = f_T\cdot\left[1+\frac{R_S+R_D}{R_{DS}}+\frac{C_{GD}}{C_{GS}+C_{GD}}\cdot g_{m0}\cdot(R_S+R_D)\right]$$

where

$$C_{GS} = \frac{C_{gs0}}{\sqrt{1-V_{gs}/V_{bi}}}, \qquad C_{GD} = \frac{C_{gs0}}{\sqrt{1-V_{gd}/V_{bi}}}$$

respectively. C_{gs0} is the zero-bias gate-source capacitance, whereas $V_{gd} = V_G - I_D R_S$ and $V_{gd} = V_G - (V_D - I_D R_D)$ are the voltage-drop across the p-n junction on either side of the channel, respectively. From the above equations, we obtain

$$f_{T0} = f_T\cdot\left[1+\frac{R_S+R_D}{R_{DS}}+\frac{g_{m0}\cdot(R_S+R_D)\cdot\sqrt{V_{bi}-(V_G-I_D R_S)}}{\sqrt{V_{bi}-(V_G-I_D R_S)}+\sqrt{V_{bi}-(V_G-V_D+I_D R_D)}}\right]$$

Since all the variables on the right hand side are directly measurable, this equation provides a simple method to extract the intrinsic f_{T0} from parasitic-limited FETs. An f_{T0} of 10 GHz was calculated for GaN JFETs using DC measurement results.

In order to estimate the ultimate speed that can be achieved in our JFETs, a calculation was made to simulate the change in g_m as L_g decreases. Figure 2 shows the calculated g_m vs. L_g curves for various saturation velocity (v_s). A 60% increase was obtained in g_m as the L_g reduced from 0.8 to 0.1 µm. By fitting the g_m of the GaN JFETs into this plot, a v_s of $6.6\text{x}10^6$ cm/s was obtained. Notice that the gate capacitance decreases linearly as the gate length shrinks. In addition, the electron velocity can exceed the v_s in ultra-short gate length FETs due to velocity overshoot under high electrical field. Considering all these effects, an f_T in excess of 50 GHz could be expected in GaN JFETs upon further improving the device design and process techniques, and scaling down the gate length. Also shown in Figure 2 were the reported g_m values of GaN MODFETs and MESFETs. The data are somewhat scattered, possibly due to different material quality for different research groups. The g_m of GaN JFET is comparable to most of them, suggesting a reasonably good quality

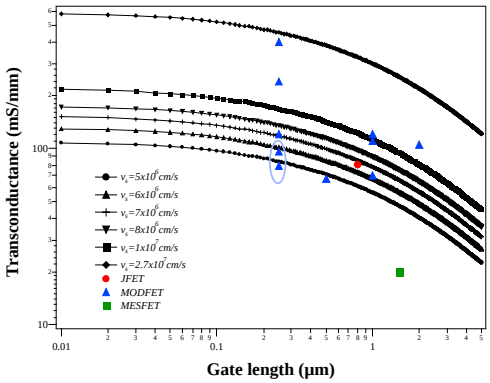

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***Figure 2**: Simulation result of g_m as a function of L_g for various v_s values. The transconductance of GaN JFETs and reported GaN MODFETs and MESFETs are also shown for comparison.*
of JFET material.

In the above analysis, the effect of non-ideal ohmic contact to p-GaN on the g_m and f_T has not been considered. For microwave operation, the large gate displacement current causes a significant voltage drop on the gate resistor, leading to a reduced g_m and f_T. In addition, the extra capacitance at metal-p-GaN interface caused by the Schottky-type Ni/Au to p-GaN contact results in a further reduction in the f_T. In order to optimize the performance of GaN JFETs, a low resistance metal contact to p-GaN with ideal ohmic I-V characteristic needs to be developed.

The DC performance of the GaN JFETs was also studied at elevated temperatures. The measurement was made on a hot plate in atmosphere. Figure 3 shows the plots of I_D and g_m as a function of V_G at different temperatures. A continuous deterioration in I_D and g_m was observed with increasing temperatures up to 200°C where the device failed after being heated in the air for ~2 hours. As the temperature was increased from 25°C to 200°C, I_D dropped from 270 mA/mm to 75 mA/mm and g_m was reduced from 48 mS/mm to 12 mS/mm, respectively. This was mainly caused by the reduction in electron mobility at elevated temperatures due to enhanced polar optical phonon scattering. However, the I_D-V_D curve exhibited an excellent pinchoff at a gate bias of –8 V, indicating a negligible gate leakage current. The failure of the JFETs after high temperature measurement was caused by the degradation of Ti/Al ohmic contact. An inspection of the devices after measurement showed a broken metal connection at the sidewall of the isolation mesa. The mesa profile was highly anisotropic, which resulted in a poor coverage of Ti/Al metal over the sidewall. Hence, the oxidation of Al upon prolonged heating in the air caused an open circuit.

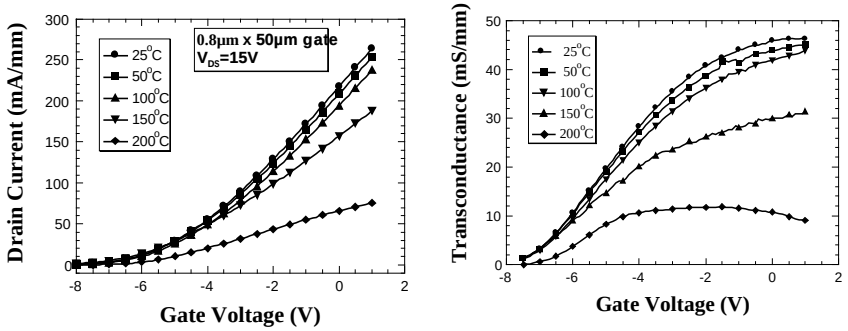

***Figure 3**: Drain current and transconductance as a function of gate voltage and measurement temperature.*

CONCLUSION

In summary, JFETs were fabricated on an epitaxially grown GaN p-n junction. These devices exhibited excellent pinch-off and a breakdown voltage that agreed with theoretical predictions. An extrinsic transconductance of 48 mS/mm was achieved with a maximum I_D of 270 mA/mm. Drain current collapse was observed in these devices after a high drain

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bias was applied due to partially depleted channel by the trapped electrons in the SI-GaN. The microwave measurement showed an f_T of 6 GHz and an f_{max} of 12 GHz. A simple method was developed to extract f_{T0} from parasitic-limited FETs. An f_{T0} of 10 GHz was calculated for GaN JFETs using DC and rf results.

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