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Charge Trapping Analysis of High Speed Diamond FETs

Pankaj B. Shah, James Weil, A. Glen Birdwell, and Tony Ivanov

Sensors and Electron Devices Directorate, US Army Research Laboratory,
2800 Powder Mill Rd, Adelphi, MD 20783, USA

ABSTRACT

Charge carrier trapping in diamond surface conduction field effect transistors (FETs) has been analyzed. For these devices two methods were used to obtain a negative electron affinity diamond surface; either plasma hydrogenation or annealing in an H_2 environment. In both cases the Al_2O_3 gate dielectric can trap both electrons and holes in deep energy levels with emission timescales of seconds, while the diamond – Al_2O_3 interface traps exhibit much shorter time scales in the microsecond range. Capacitance-Voltage (CV) analysis indicates that these interface traps exhibit acceptor-like characteristics. Correlation with CV based free hole density measurements indicates that the conductance based interface trap analysis provides a method to quantify surface characteristics that lead to surface conduction in hydrogenated diamond where atmospheric adsorbates provide the acceptor states for transfer doping of the surface.

INTRODUCTION

Group III-nitride electronics have demonstrated a substantial scale up of power and frequency performance over that of GaAs and other high frequency material systems. However, as these devices are tasked in challenging high power RF applications, we are seeing limitations due to heat generation and removal. Advance techniques to mitigate this are still challenged by the thermal interface resistance between the active region semiconductor material and other heat removal layers. This interface resistance is dominated by defects at the interfaces affecting phonon transport and scattering. [1] One way to overcome these thermal limiting issues is to move to a new semiconductor material, and diamond appears to be the best candidate.

Diamond's high thermal conductivity, large breakdown field and high carrier mobility offer are its strengths. [2] Given the large ionization energies of bulk dopants in diamond, we are instead considering surface conduction devices. These are formed using a hydrogenated diamond surface which exhibits a negative electron affinity that aligns the valence band with acceptor states in an adjacent surface layer material. With the resulting migration of electrons from the diamond surface, a hole conduction channel is formed in the diamond region near the surface. High quality p-channel diamond FETs when paired with n-channel GaN FETs would offer complementary pairs for in power electronics. Organizations have already demonstrated that this conducting channel is a 2D hole gas. [3] For high frequency applications, the device turn-on must also be fast. In this work we describe the transient performance of our transfer doped diamond FETs. Charge carrier trapping is analyzed and related to device properties.

EXPERIMENT

For this work high grade single crystal diamond wafers 3 mm × 3 mm were obtained from Element6. A two-step chemical clean was performed beginning with a 45 minute soak in a 150

°C solution of HCl: HNO_3 having a 3:1 ratio followed by a 45 minute soak in a 150 °C solution of H_2SO_4: HNO_3 having a 3:1 ratio. This clean process also oxidized the surface. Then surface hydrogenation was performed using two methods. One wafer was annealed for 30 minutes at a substrate temperature of 850 °C in a 700 Torr H_2 atmosphere. The other was exposed to a hydrogen plasma for 60 minutes during which the wafer temperature was 800 °C. In these FETs atmospheric adsorbates on the hydrogenated diamond surface act as transfer dopants.

After hydrogenation a typical FET fabrication procedure using four mask levels was followed starting with gold deposition to protect the hydrogenation over what will become the active region with liftoff of the gold to expose diamond in regions between individual devices. The wafer was then exposed to an oxygen plasma under low power (100 W) for 30 seconds to oxygenate the surface for device isolation. Next the gold was etched to form individual source and drain pads of the FETs using a KI/I solution which left a roughly 1.5 micron undercut below the resist mask. Using the same resist mask, a 160 angstrom thick Al_2O_3 layer was electron-beam evaporated forming a gate dielectric on which an Al/Au gate contact layer was deposited.

All electrical measurements were performed in the dark on a Cascade Microtech, Summit 12000 AP probe station with PureLine enhanced EMI shielding and triax connections to the probe tips and a guard that completely surrounds the wafer. All electrical data was taken using an Agilent B1500 Parametric Analyzer. Effective mobility was measured by calculating the charge under the gate utilizing a CV measurement.

DISCUSSION

Both hydrogenation processes led to FETs with typical output characteristics as shown in figure 1(a) for the wafer hydrogenated by annealing in an H_2 environment. Transient switching was analyzed for this FET leading to the results in Fig 1(b). Here we show the slow turn-on

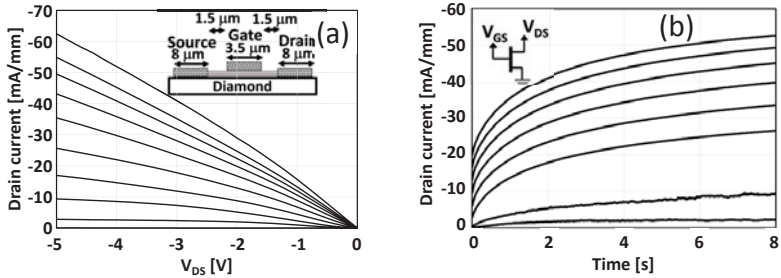

Figure 1. (a) Output characteristics of this diamond FET hydrogenated with an H_2 environment anneal. V_{GS} = 0 (lower) to -8 V (upper) curve in 1 V increments. (b) Pulsed turn-on I_D transients following a 10 second soak at a quiescent bias of (V_{GSQ}: V_{DSQ}) = (4V, -10V) to on-state bias of (V_{GS}: V_{DS}) = (-6: -1, -2, -3, -4… -8).

that is usually associated with current collapse plots as has also been seen in III-nitride HEMTs. [4] Here the transistor is pulsed following a soak for 10 seconds at a quiescent bias of (V_{GSQ}: V_{DSQ}) = (4V, -10V) to on state (V_{GS}, V_{DS}) points along the -6 V V_{GS} curve of figure 1(a). A slow rise time of over 6 seconds is seen. We also observe a large jump between the V_{GS} = -2 V curve and the V_{GS} = -3 V curve and in some cases see large discrete jumps during a single gate

bias transients. These jumps are similar to the cause of burst (random telegraph signal) noise seen in low frequency noise measurements and indicates that there may be a large population of trap states at a few discrete energy levels.

For the FETs formed on the plasma hydrogenated wafer, the turn-on transients were not as smooth as is shown in figure 2. Shown here are turn on transients following an 8 second soak at four different quiescent bias conditions. Compared to pulsing on from the quiescent bias of (V_{GSQ}, V_{DSQ}) = (0,0), when first applying for 8 seconds a quiescent bias of (V_{GSQ}, V_{DSQ}) = (4, -6) the gate is held at a more positive bias for a while during which holes are injected from the gate contact into the Al_2O_3 gate oxide where they are trapped. When the device is then turned on, these trapped holes slowly leave the deep traps where they act as a virtual gate, and as they do the current flow increases as seen in the current transients. Figure 2 also shows greater effects of the random telegraph signal like trapping and detrapping of charges in the gate oxide during turn-on. The plasma hydrogenated wafer also exhibited poor turn-off performance.

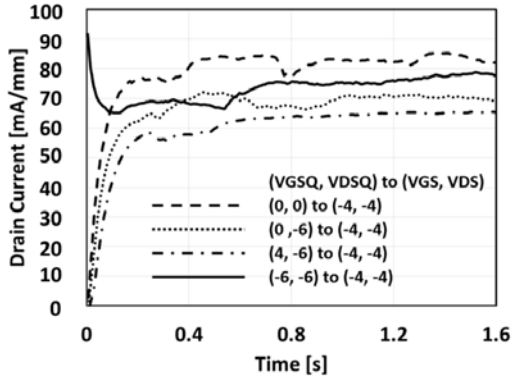

Figure 2. Pulsed switching for a plasma hydrogenated diamond FET from different quiescent bias conditions. Measurement conducted at a chuck temperature of 15 °C

The CV measurement taken at a 1 MHz signal frequency shown in figure 3 indicates that electrons can also be trapped in the Al_2O_3 gate oxide. This plot was obtained by first biasing the gate for 30 seconds at -4 V relative to the ohmic contacted channel, and then ramping the gate bias up to +8 and back within 20 seconds. For these measurements the flat-band voltage should be close to 0.22 V which is the difference between the work function of the aluminum gate (4.08 eV) and the valence band energy level of the hydrogenated (100) diamond surface (4.3 eV). What we observe is that the 30 second negative gate bias injects electrons into deep traps in the Al_2O_3 and this negative charge causes the flat band to be at a much more positive bias. Then as the gate bias reaches 8 V and starts ramping negative the channel turns on and higher conduction starts. This higher conduction (seen in the dashed conductance peaks) helps neutralize the charge in the gate causing the flat band voltage to match the theoretically expected value of 0.22 V. Therefore along with the deep hole traps discussed above, the Al_2O_3 dielectric also exhibits deep electron traps. When the CV curves are measured starting with a 30 second soak at +8 V (not shown here), there was less hysteresis because as before when ramping from 8 to -4 V there is high conduction causing the flat-band to be close to 0.22 V. Then, as the bias switches direction and ramps back to 8 V, the short time that the negative bias was applied led to less

electron injection and trapping in the Al_2O_3 compared to that shown in figure 3. The long time constants of figure 1, 2 and 3 indicate deep traps in the Al_2O_3 layer. We believe that this e-beam evaporated Al_2O_3 is amorphous as is seen in other similarly deposited samples. [5] From the CV measurement we estimate that the dielectric constant of the Al_2O_3 layer is 7.2 eV which is similar to values reported by other groups. [6]

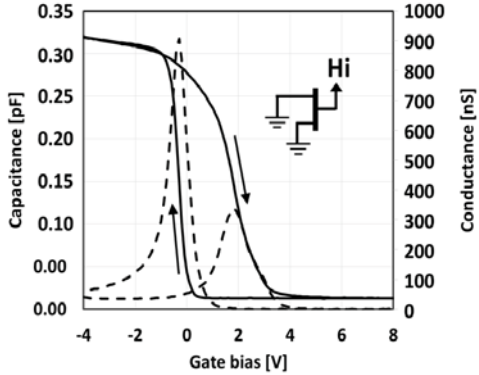

Figure 3. Capacitance (solid line) and conductance (dashed line) plots for an H_2 annealed diamond FET with gate length 3.5 micron and width 80 micron. V_{GS} was held at -4 V for 30 seconds before the ramp to V_{GS} = 8 V and back.

Interface trap analysis of the Al_2O_3 / hydrogenated diamond interface, correcting for series resistance of the contacts and access regions, [7] indicated good band bending efficiency [8] as shown in figure 4(a) and a higher trap density in the FET hydrogenated by an H_2 environment anneal as shown in figure 4(b). These traps are shallow as indicated by the ionization energy level which is limited

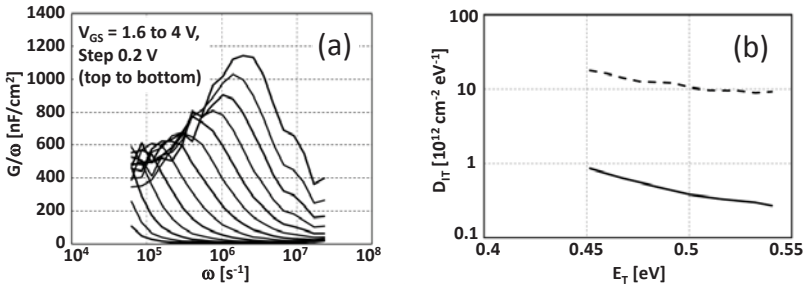

Figure 4. The hydrogenation using H_2 anneal FETs (a) conductance vs. radial frequency data obtained from the interface trap analysis and (b) interface trap density for the H_2 annealed FET (dashed) and the plasma hydrogenated FET (solid)

by the frequency of the CV meter. For these calculations a capture cross section of 4×10^{-13} cm^2 was used, [9] though little error arises from variations in this number. Also, we used 2.7×10^{-19}

cm^{-3} for the effective valence band density of states. [10] The trap time constant also exhibited a nearly exponential dependence on gate bias.

Capacitance voltage measurements at different frequencies shown in figure 5 indicates that at lower frequencies the flat-band voltage of these curves shift to the right. The right shift is due

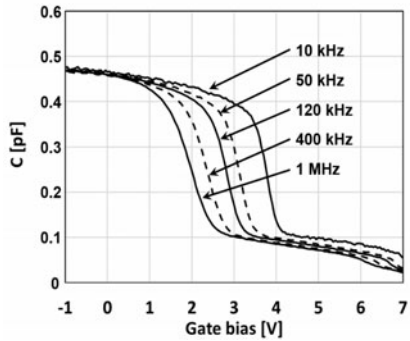

Figure 5. CV data measured at different signal frequencies for the FET hydrogenated by an H_2 environment anneal.

to increased trapping of negative charges in acceptor type traps as the signal frequency reduces. We surmise that the acceptor traps quantified here may be those providing the energy levels for electrons to migrate to from the diamond surface leading to transfer doping and hole gas formation. This is because there is a direct correlation between the trap density in figure 4(b) and the channel charge density obtained from CV measurements as shown in figure 6(a), and

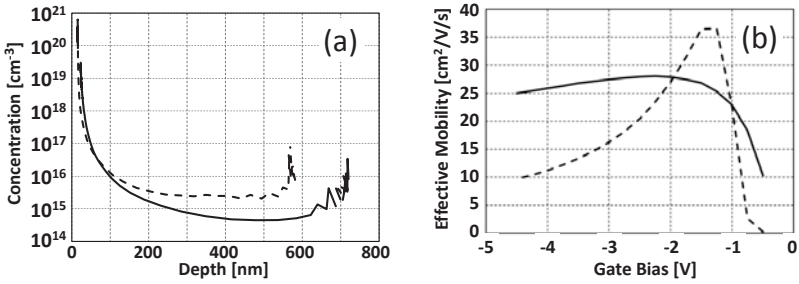

Figure 6. (a) CV measurement extracted free hole density of the FET hydrogenated by an H_2 anneal (dashed) and by hydrogen plasma exposure (solid line). The corresponding effective mobility is shown in (b).

because a completely hydrogenated diamond surface should not have any surface states. In figure 6(a) we see that hydrogenation by annealing in H_2 lead to a higher hole density than plasma hydrogenation with values comparable to those reported in the literature for hydrogenated diamond FETs. [11] The free hole density in the FET hydrogenated by annealing in H_2 is 1.5×10^{13} cm^{-3} and in the plasma hydrogenated FET is 4.9×10^{12} cm^{-2}. Also, the 2D electron gas depth from the surface was 16 nm for the hydrogenation by H_2 anneal case and 23

nm for the plasma hydrogenation case. Furthermore, the plasma hydrogenated FET depletes further into the diamond which may explain its poor turn-off performance. In the cases under consideration here we still need to analyze hydrogen coverage and quantify defects and inclusions that affect the actual surface state density. Also, roughening of the surface and other issues resulting from the hydrogenation process may affect the quality of the FET gate dielectric layer deposited on top of the surface conduction channel, further influencing device performance. From an effective mobility measurement of the transistor we obtain the values shown in figure 6(b) for the two hydrogenation cases. We observe that while operating in saturation the plasma hydrogenated FET exhibited higher mobility but lower free carrier concentration. Thus both FETs had very similar on currents in saturation.

CONCLUSIONS

Using two different techniques to hydrogenate diamond for surface channel FETs, plasma hydrogenation and annealing in an H_2 environment, we have investigated charge carrier trapping in the gate dielectric and at the interface. These FETs were transfer doped using atmospheric adsorbates and the conductance method for interface trapping could identify the acceptor characteristics indicating that this method would provide a metric for analyzing the transfer doping. Also, trapping of both electrons and holes into deep traps in the Al_2O_3 gate dielectric with time constants in the range of seconds was observed in quiescent bias switching and CV hysteresis measurements. Comparable drain current levels in the saturation region of the FET output characteristics indicate similar hydrogenation coverage of the surface by the two techniques used; however, free carrier concentration and mobility should be individually observed when optimizing the hydrogenation technique.

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