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Etching Dynamics of Geometrically Confined Silicon Nanostructure

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Currently, semiconductor fabrication process is extremely shrunken in size and became intricated to form denser integrated circuits. As the size of the element within the transistor approaches to the width of several atoms, structure fabrication is facing unprecedent challenges. Among the multiple stages of device formation, chemical wet etching is a fast and low temperature process for removing unwanted material with high selectivity [1, 2]. However, the etching rate of material is significantly reduced compared to the bulk condition and stopped when it is surrounded by the dielectrics. This slow etching and unstripped debris became one of the major obstacles during the metallized gate and need to be conquered for the next generation processing node.

Liquid-phase transmission electron microscope (LPTEM) is a promising technique for observing materials in the liquid with a resolution of nanometers. Growth and assembly of the nanoparticles, dynamics of electrochemical reactions, catalytic reaction, and the structure of wet biological materials is previously revealed with various liquid cell configurations [3]. Aabdin *et al*., have previously reported wet etching process of uncovered amorphous Si pillars using LPTEM, which has potential application to 3D semiconductor nanostructures [4]. Yet the actual semiconductor process nodes usually require the etching of nano-confined silicon patterns.

Herein, we have first demonstrated wet etching processes of exposed and confined crystalline Si using LPTEM. Crystalline Si nanowires with diameter of 20 nm were rinsed with 0.5 wt% of HF solution to remove native oxide on the surface. Then, they were drop casted on SiN_x e-chip with the heater element and assembled to the liquid TEM holder (Poseidon Select, Protochips, USA). For the confined nanowire, 50 nm of tetraethyl orthosilicate (TEOS) silicon oxide is deposited upon the Si nanowire with the gas injection system of focused ion beam (FIB) before assembling. Finally, 10 % (w/w) of TMAH solution is filled into the liquid cell with the syringe pump and heated up to 50 ℃, which is the actual semiconductor process wet etch temperature. The time-series TEM image of etching process of uncovered Si nanowires are shown in **Figure 1**. The nanowire was etched in radial direction rather than the longitudinal direction, forming islands during the etch. However, when the nanowire is passivated with the TEOS oxide materials transport is significantly reduced and unetched Si nano-islands are trapped inside of the cavity (**Figure 2**).

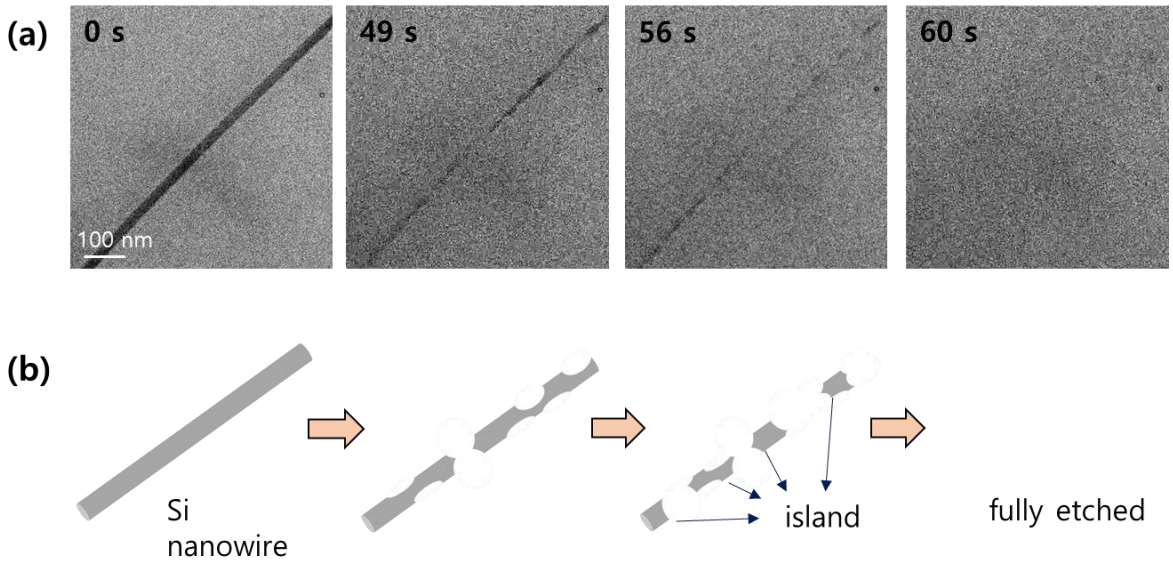

Figure 1. (a) Real-time TEM images showing etching process of exposed Si nanowire. (b) schematic diagram of detailed explanation of (a).

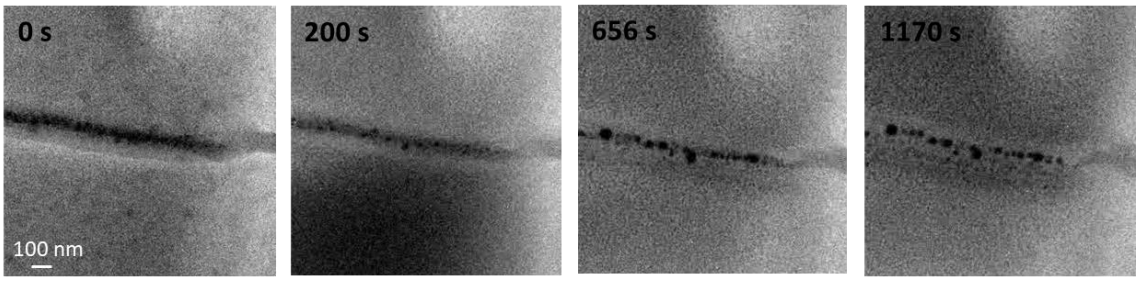

Figure 2. Real-time TEM images showing etching process of confined Si nanowire

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