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Broadband packaging solution in embedded wafer level ball grid array technology for D-band PMCW radar

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Abstract

A system-in-package for a wideband digital radar, in D-band, requires broadband, high-gain antennas combined with broadband chip-to-package and package-to-printed circuit board (PCB) interconnects. This paper demonstrates a wideband, low-loss quasi-coaxial signal transition, and a novel electric split ring resonator (eSRR)-based antenna-in-package (AiP) with a modified reflector concept, for improved gain, in embedded wafer level ball grid array (eWLB) technology. A complete chip-to-package-to-PCB interconnect is also demonstrated by combining the quasi-coaxial transition with a chip-to-package interconnect. The quasi-coaxial signal transition has the largest impedance bandwidth among ball grid array-based quasi-coaxial signal transitions. For the modified reflector concept, a horn-shaped cavity is micromachined in the PCB substrate and remetallized with aerosol-jet printing, placing the reflector 0.25λ from the antenna. The antenna gain is improved with up to 5.3 dB. The AiP with the horn-shaped reflector is the single element with the highest gain, in eWLB technology, above 100 GHz.

Introduction

Recently, there has been a drive to release additional parts of the spectrum above 116 GHz for novel sensing applications [1]. With the large amount of bandwidth available at these frequencies, such as in D-band for instance, radars with an ever greater range resolution is achievable and due to the short wavelength, the radar can be very compact. This makes it easy to integrate the sensor into different devices for a new generation of touchless, intuitive human–machine interactions. In this context, the components detailed in this work have been tailored for a broadband, 140 GHz radar transceiver. While their application is versatile, the specific motivation behind their development centered on their integration with a 140 GHz phase-modulated continuous wave (PMCW) radar, designed to offer a 12.5 GHz baseband bandwidth, specifically for hand gesture recognition [2, 3].

Naturally, radar sensors for hand gesture recognition, at such frequencies, are not without their challenges. Constraints on transmitter power, receiver sensitivity, and significant free space path loss at 140 GHz are among these obstacles. The nature of the target, a moving hand performing complex gestures, also dictates certain system requirements. To compound the problem, it has been determined that the radar cross-section of a human hand can be as low as −45 dBsm [4], although it depends on the gesture. These challenges necessitate antennas with sufficiently high gain.

Excellent range resolution is also required to be able to distinguish between small targets. In radar systems, the range resolution improves with an increase in the bandwidth. In PMCW radar specifically, the bandwidth is directly proportional to the sampling rate of the chosen pseudorandom binary sequence [5]. Elevated sampling frequencies, necessitates a higher clock frequency and an increased analog-to-digital converter output sampling rate. Therefore, for fine range resolutions, the interconnect between the packaged transceiver and the field programmable gate array (FPGA) will require an expansive bandwidth. Additionally, for the aforementioned PMCW radar, the voltage-controlled oscillator (VCO) will be off-chip, residing on the printed circuit board (PCB). Positioning the VCO on the PCB enables the use of standard, off-the-shelf VCOs typically having higher output power. A high-power VCO greatly enhances the signal-to-noise ratio. Heat management is also more straightforward on the PCB, through the use of large heat sinks. For the D-band radar discussed above, the VCO operates at 35 GHz; thus, future radar applications at higher frequencies will require proportionally higher VCO frequencies.

Therefore, one can conclude, high-gain, broadband antennas combined with broadband chip-to-package and package-to-printed circuit board (PCB) interconnects are required for PMCW radars with a high sampling rate. This work presents a broadband packaging solution within the D-band, using embedded wafer level ball grid array (eWLB) technology. Two crucial components required for a wideband system-in-package (SiP) are demonstrated for the first time in eWLB technology: a wideband, low-loss quasi-coaxial signal transition, and an innovative electric split ring resonator (eSRR)-based antenna-in-package (AiP) featuring an enhanced reflector design for superior gain. Subsequent sections provide a concise overview and comparison with contemporary eWLB antennas and ball grid array (BGA)-based quasi-coaxial interconnects.

AiP in eWLB

Embedded wafer level ball grid array (eWLB) technology is a favorable packaging technology for millimeter-wave systems due to a variety of reasons [6]. A key advantage is the minimization of package loss due to compact microvias forming the monolithic microwave integrated circuit (MMIC)-to-package interconnects, and the mold compound exhibiting a stable dielectric constant and a low loss tangent, above 100 GHz. Additionally, antennas and signal lines can be realized in a redistribution layer (RDL) with excellent precision and resolution. Figure 1(a) shows a simplified cross-section of a standard eWLB package.

Several antennas have been realized in eWLB at 60 GHz [7] and 77 GHz [8, 9]. However, designs beyond 100 GHz are limited. The 120 GHz differential bow-tie and a 240 GHz single-ended slot-type bow-tie from [10] are of note. To date, the antennas in [10] have the highest bandwidth of eWLB antennas, above 100 GHz. Regarding wideband antennas centered around 140 GHz, a single-ended corner patch element from [11] and results for a dipole, bow-tie, and rhombic differential antenna [12] have been published. The round SRR antenna from [13] and the differential, square SRR (SSRR) antenna from [14] are significant contributions in this area. The SSRR had the highest gain, for a single antenna element, in eWLB packaging technology, above 100 GHz, to date. The work presented here is an extension of work first presented in [14].

Despite the fact that the reflector on the PCB has a significant impact on the antenna gain in an eWLB package, possible improvements related to the reflector, remain unexplored. Typically, a planar reflector, placed 0.1λ (at 140 GHz) from the antenna, is used. This antenna-to-reflector distance is fixed by the size of the solder balls used in a BGA and the parameters used in a reflow soldering process. This work introduces a differential electric SRR (eSRR) antenna with augmented gain via a cavity micro-machined and re-metallized in the PCB substrate. The horn-shaped reflector is set at a $\lambda/4$ distance from the eWLB antenna. The horn-shaped reflector concept, combined with an eWLB AiP, is shown in Fig. 1(b). To the best of the authors' knowledge, a differential eSRR AiP, with a horn-shaped reflector, which improves the peak gain by roughly 2.3 dB, is demonstrated here for the first time. The modified package concept results in a single antenna element with a peak gain surpassing that of [14], and is thus the highest to date.

BGA-based quasi-coaxial interconnects

Several published works have explored BGA-based quasi-coaxial interconnects. Shao et al. [15] introduced a broadband transition between a substrate integrated coaxial line (SICL) in low temperature co-fired ceramic (LTCC) technology, and BGA-based interconnect quasi-coaxial interconnect. The insertion and return loss results for the full back-to-back transition is obtained with a hybrid model, by cascading the measured SICL component, with the simulated parameters of the BGA transition. The tin BGA balls are assumed to have a diameter of 400 μm and height of only 100 μm. A DC to 35 GHz broadband interconnect in high temperature co-fired ceramic (HTCC) technology is presented in [16]. The structure connects two transmission line sections in HTCC, via a BGA-based quasi-coaxial transition. Likewise, in [17], a quasi-coaxial transition between two composite boards is realized in BGA. A coaxial BGA layout is also demonstrated in [18], to connect a HTCC substrate to a PCB for a broadband RF multi-chip SiP packaging module. In [19], a vertical quasi-coaxial interconnect connects two substrates, for use in 3-D SiP modules, at 60 GHz. The interconnect uses copper balls with a diameter of 350 μm, attached with solder paste to the upper and lower substrates. The single copper ball for the signal line is surrounded by six copper balls, forming the ground connection. A back-to-back prototype with CPW feed lines on the lower substrate and a CPW through line on the upper substrate, was manufactured. The quasi-coaxial interconnect in [19] is improved in [20], by forming an excavated structure to minimize fluctuation in the positions of the copper balls during the reflow process. A complex structure consisting of a stacked strip-line-to-quasi-coax and quasi-coax-to-GCPW transition, connecting 3 multi-layered substrates is shown and fabricated. In [21], a vertical quasi-coaxial connection is used to connect a chip to an external V-band waveguide through a fenced stripline in a multi-layer LTCC package. The flip chip bumps have a diameter of only 75 μm.

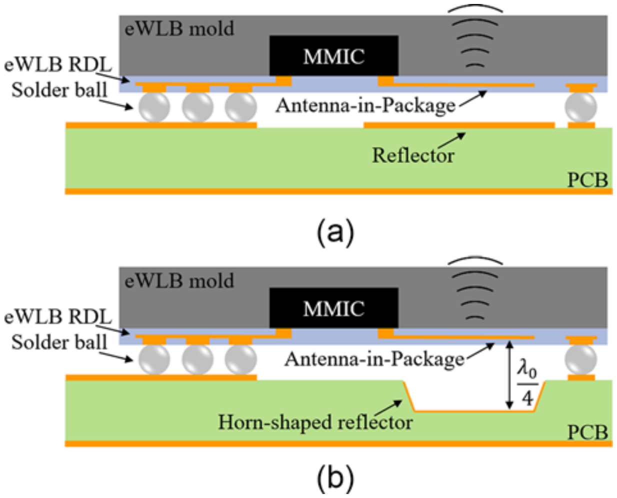


Figure 1. Simplified schematic of the cross-section of an eWLB package: (a) standard and (b) with a horn-shaped reflector.

A wideband 140 GHz PMCW radar SiP necessitates broadband interconnects from chip-to-package and package-to-PCB. In this paper, a DC to 100 GHz quasi-coaxial signal transition is demonstrated in eWLB technology for the first time. The quasi-coaxial transition presented here has a return loss of greater than 10 dB, up to 103 GHz. Its insertion loss is less than 0.6 dB per transition, up to 80 GHz, and less than 2.2 dB, up to 100 GHz. From the excellent measured return loss and insertion loss values, one can conclude, a 50 Ω impedance is maintained as closely as possible throughout the chip-to-package-to-PCB interconnect. To the best of the authors' knowledge, this eWLB-based quasi-coaxial signal transition exhibits the largest impedance bandwidth compared to the various published BGA-based quasi-coaxial interconnects, without requiring a special manufacturing technology (see Table 2). For context, the upper cutoff frequency for a 1 mm air coaxial connector, operating in its fundamental transverse electromagnetic (TEM) mode, is roughly 130 GHz, and these connectors are used up to 110 GHz. The quasi-coaxial signal transition demonstrated in this work closely approaches this limit, while considering eWLB manufacturing constraints. A full chip-to-package-to-PCB interconnect is also shown, in which the eWLB-based quasi-coaxial signal transition forms the package-to-PCB interconnect, and an on-chip through-line fabricated in 22-nm fully depleted silicon on insulator (FDSOI) CMOS technology is used to form the chip-to-package interconnect. These interconnects are realized in a back-to-back or daisy chain configuration, which enables probe-based S-parameter measurement.

The remainder of the paper is structured as follows. Section "Design" provides details on the design of the quasi-coaxial signal transition, the eSRR antenna and its horn-shaped reflector. In the "Manufacturing and assembly" section, the manufacturing of the horn-shaped reflector and the assembly of the packages are discussed. The results are presented in "Results" section, and the paper is concluded in last section.

Design

In this section, the design of the quasi-coaxial signal transition will be discussed first, followed by the design of the eSRR antenna and the horn-shaped reflector.

Chip-to-package-to-PCB interconnect

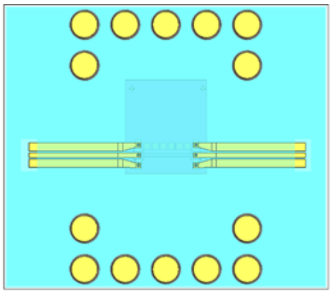
Three different interconnect structures are demonstrated in this paper, namely, a chip-to-package, a package-to-PCB and a chip-to-package-to-PCB interconnect. All interconnects are demonstrated in a daisy chain/back-to-back configuration to enable probe-based S-parameter measurement.

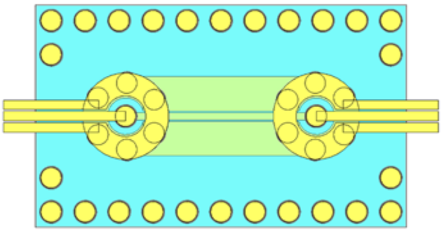
A chip-to-package interconnect realized by means of eWLB microvias is shown in Fig. 2(a). The design consists of ground plane taper connecting the RF pads on the chip, with a pitch of 125 μm, to the 50Ω CPW line in the RDL layer of an eWLB package. The on-chip through-line is fabricated in 22-nm FDSOI CMOS technology.

The package-to-PCB interconnect, realized by means of a quasi-coaxial signal transition (see Fig. 2(b)), is designed as follows. The first step in the design of the quasi-coaxial signal transition is to calculate the theoretical characteristic impedance of the quasi-coaxial signal transition, with the following equation from [22], for the impedance of a coaxial transmission line:

$$Z_{\text{coaxial}} = \frac{60}{\sqrt{\epsilon_r}} \ln\left(\frac{r_{\text{outer}}}{r_{\text{inner}}}\right). \quad (1)$$

As the BGA-based quasi-coaxial signal transition is air-filled, $\epsilon_r = 1$. The solder balls of the packages demonstrated in this paper in eWLB technology, have a standard pitch of 500 μm and diameter of 375 μm – see [6, 23]. This leads to an initial calculation of $Z_{\text{coaxial}} = 31\,\Omega$ for the quasi-coaxial signal transition. The quasi-coaxial transition supports the TEM mode. The cut-off frequency of the TE_{11} mode of a standard coaxial transmission line can be estimated with the following equation,


(a)


(b)

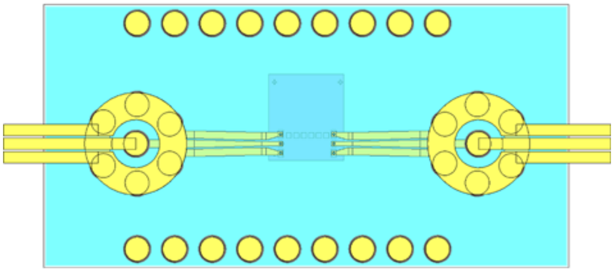

(c)

Figure 2. Interconnect design (shown without PCB substrate): (a) chip-to-package; (b) package-to-PCB; and (c) complete chip-to-package-to-PCB.

$$f_{\text{TE}_{11}} = \frac{c}{\pi\sqrt{\epsilon_r}(r_{\text{outer}} + r_{\text{inner}})}. \quad (2)$$

The cut-off frequency, for the initial design values mentioned above, is $f_{\text{TE}_{11}} = 139$ GHz, if one assumes r_{outer} to be defined as the pitch of the solder balls. This is more than sufficient for the proposed PMCW radar SiP application.

The position of the solder balls, the size of the ground ring on the package and on the PCB, as well as the width of the finite ground plane in the package, is subsequently optimized in CST Studio Suite software – taking into consideration, the design rules of the eWLB manufacturing technology. The simulation model for the optimization process can be seen in Fig. 3(a) – two waveguide ports are placed on either side of the quasi-coaxial signal transition. The insertion and return loss for the optimized signal transition model is given in Fig. 3(b). The characteristic impedance of the optimized quasi-coaxial signal transition is calculated with [24]:

$$Z_c = Z_0\sqrt{\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}}. \quad (3)$$

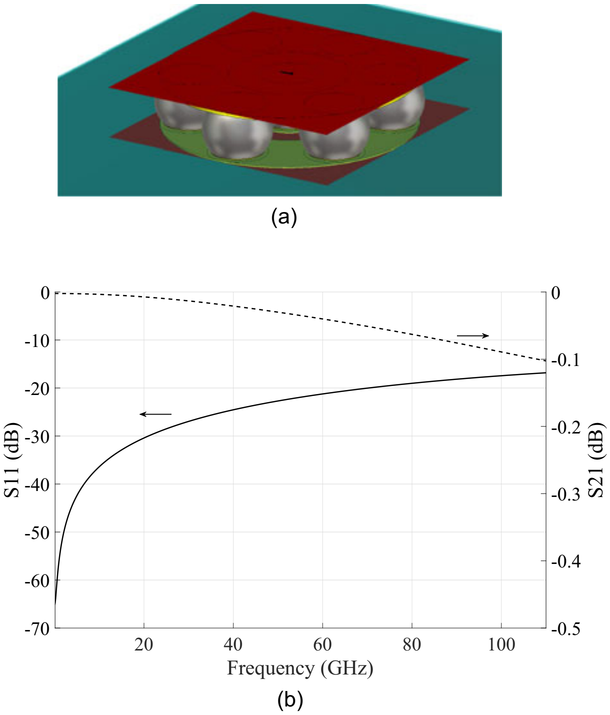


Figure 3. Quasi-coaxial signal transition: (a) simulation model for optimization and (b) simulation results.

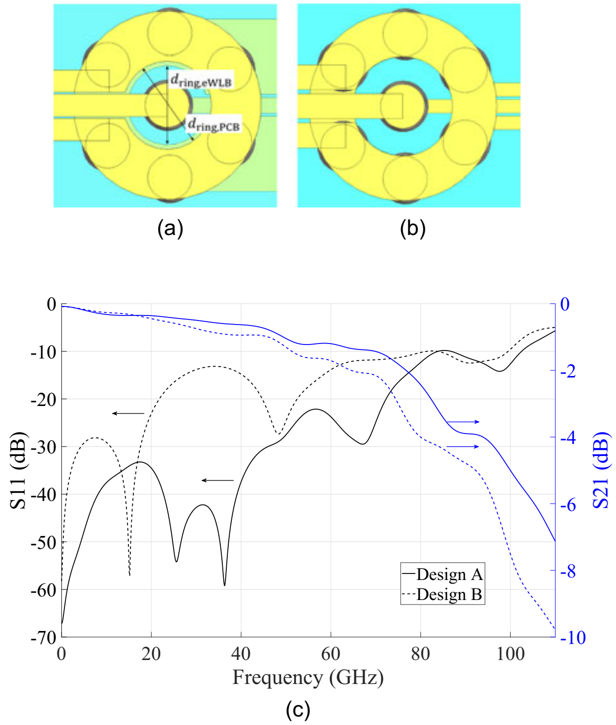


Figure 4. Two models of the quasi-coaxial signal transition: (a) Design A; (b) Design B; and (c) comparison of results.

Using Eq. (3), the characteristic impedance is calculated as 40.3 Ω, at a center frequency of 55 GHz. Thereafter, the quasi-coaxial signal transition is connected to 50 Ω CPW lines on the package and PCB.

Two models for the quasi-coaxial signal transition are presented here – Design A (Fig. 4(a)) and Design B (Fig. 4(b)). Design A has been optimized to ensure minimal return and insertion losses over an expansive bandwidth. Contrarily, Design A is characterized by an extended ground plane and reduced inner ground ring diameter compared to Design B, with $d_{\text{ring, eWLB}} = 0.576$ mm, $d_{\text{ring, PCB}} = 0.64$ mm. Design B boasts a more compact footprint, but it incurs a marginally higher insertion loss in comparison with Design A. Design B has a more compact footprint, with narrower ground planes, but it incurs a marginally higher insertion loss in comparison with Design A. The inner diameter of the ground ring on the package is also larger for Design B – $d_{\text{ring, eWLB}} = d_{\text{ring, PCB}} = 0.72$ mm. Furthermore, Design B seamlessly integrates with the chip-to-package interconnect presented earlier. Nonetheless, both Designs A and B of the quasi-coaxial signal transition remain viable options; using Design A would merely necessitate adjusting the chip-to-package interconnect to accommodate the broader ground plane. The return and insertion loss of the back-to-back quasi-coaxial-to-CPW signal transition, with a CPW line 1.65 mm long connecting the two quasi-coaxial transitions, are shown in Fig. 4(c), for both designs. A back-to-back model of Design A of the quasi-coaxial signal transition is manufactured, to illustrate the wideband characteristics of the eWLB-based quasi-coaxial signal transition for the first time.

Lastly, the quasi-coaxial signal transition given in Fig. 4(b) (Design B) is used in the design of the full back-to-back chip-to-package-to-PCB interconnect – see Fig. 2(c) – due to ease of integration and the smaller area requirement. All the interconnects presented in this section use RO4003C, with a thickness of 508 μm as PCB substrate.

eSRR antenna

The design of the eSRR antenna is based on electrically resonant terahertz metamaterial unit cells originally proposed in [25, 26]. Unlike classic SRRs, whose electric and magnetic responses are strongly coupled (resulting in a complex magnetoelectric response), eSRRs have a pure electric response [25]. The symmetrical structure of an eSRR eliminates the magnetoelectric response by counter-circulating currents in the unit cell. Figure 5 shows the design and dimensions of the novel, uniaxial, differential eSRR antenna, that is demonstrated in this paper for the first time. The width of the strip closest to the feed was increased to improve the matching and return loss. The antenna is square, with $l_1 = 0.27\lambda_g$ (λ_g is the guided wavelength) and when including the surrounding finite ground conductor, $l_2 = 0.48\lambda_g$. The antenna is realized in an eWLB package of 4×5 mm^2.

The antenna has a 100 Ω coplanar strip line (CPS) for its feed. A probe-based antenna measurement setup is used [27] to characterize D-band antennas from 110 to 170 GHz. For D-band measurements, single-ended probes are used, therefore, a balanced-to-unbalanced (i.e. balun) transition is required when measuring differential antennas. A Chebyshev quarter-wave stepped balun transformer is used for the 50 Ω CPW to 100 Ω CPS transition – previously characterized in [12]. This balun necessitates bond wires to bridge the finite ground planes. The bond wires are added manually during the assembly process. Two bond wires are added on both sides of the radial slot. The balun's intended application is solely for the antenna characterization, and considering that MMICs frequently adopt differential outputs, it is

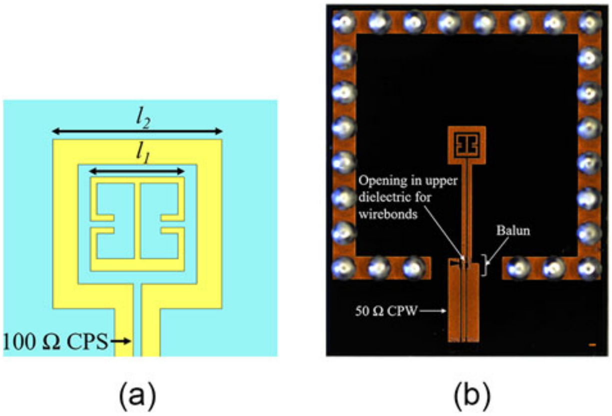


Figure 5. eSRR antenna: (a) simulation model with dimensions and (b) microscope photo of a prototype.

not intended for integration into future products. A microscope photo of the differential eSRR antenna prototype, with the aforementioned Chebyshev balun, in the eWLB package, is shown in Fig. 5.

As can be seen from Fig. 1(a), the antenna's radiation is reflected by the reflector realized on the PCB and therefore radiates through the mold, in the direction opposite of the feedline and probe. In this paper, a simple change is introduced in the conventional eWLB-package-and-PCB assembly, which enhances the gain of an eWLB AiP significantly. Due to the height of the solderballs after soldering and assembly, the usual distance between the antenna and reflector, is approximately 0.1λ, at 140 GHz. By simply increasing the distance between the eWLB AiP and a PCB-based reflector, to 0.25λ, constructive interference of the electric fields should result in a higher antenna gain. Therefore, 290 μm is additionally required between the antenna and the reflector – this is used as the initial value for the depth of the horn-shaped reflector. This idea leads to the proposed modified package concept illustrated in Fig. 1(b), where a horn-shaped reflector is manufactured in the PCB, instead of a planar reflector as was custom in previous publications [11]–[14].

Of course, a smooth horn is difficult to realize in alumina substrate. The horn ramp is approximated with steps of 20 μm – see Fig. 6(b). A VBA macro is used to model the layers in CST. It was determined in simulation that as long as the steps are less than 25 μm in height, the AiP performance is similar to that of the simulation model using a smooth horn (Fig. 6(a)). It is further determined, through optimization in CST Studio Suite software, that a slope of 15°, and a horn aperture of $2.5 \times 2.5\ \text{mm}^2$ results in an optimum gain value, and a horn height of 260 μm leads to the highest average gain from 130 to 150 GHz. The total substrate thickness of the alumina in which the horn-shaped reflector is realized, is 508 μm – a standard sheet thickness.

In Fig. 7, the return loss and the gain of the eSRR antenna, with three different reflectors, are presented – two planar reflectors and the horn-shaped reflector described above. The results for two different planar reflectors are presented – for an antenna with a Rogers 4003C substrate and an alumina substrate. In both cases, the PCB substrate is 508 μm thick with a $2.25 \times 2.25\ \text{mm}^2$ reflector on the PCB. The RO4003C simulation results are included here, to ease comparison with prior works [11]–[14] that used a similar substrate. The impedance bandwidth of the three different scenarios are similar – the reflection coefficient is below −10 dB from 127 to 166 GHz (a relative bandwdith of 26.9%). The gain, however, improves quite significantly, with the antenna with the horn-shaped reflector exhibiting a peak gain of 10.2 dBi – an improvement of 2.3 dB from the case of the planar reflector. A significant improvement is especially noticeable at the higher frequencies – an improvement of up to 5.3 dB can be seen around 149 GHz.

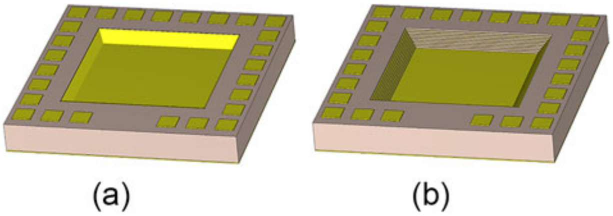


Figure 6. Simulation models of horn-shaped reflector of eSRR antenna: (a) simplified model of smooth horn and (b) horn shape approximated by metallized steps.

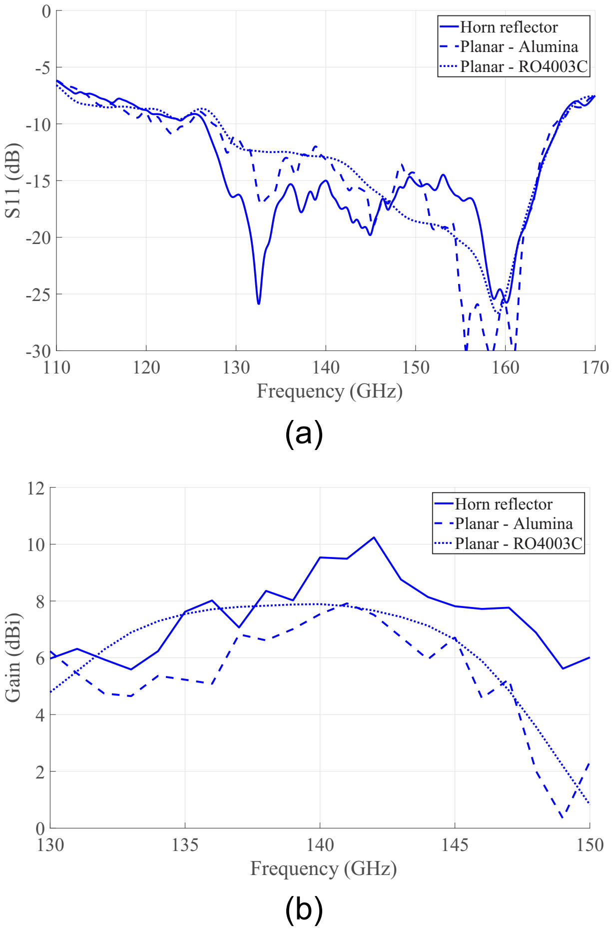


Figure 7. Simulation results of eSRR antenna with different reflectors: (a) reflection coefficient and (b) antenna gain.

Manufacturing and assembly

The eWLB packages of the antenna and interconnect prototypes are manufactured by Infineon AG. Microscope photos of the manufactured prototypes of the interconnects can be seen in Figs. 8(a),

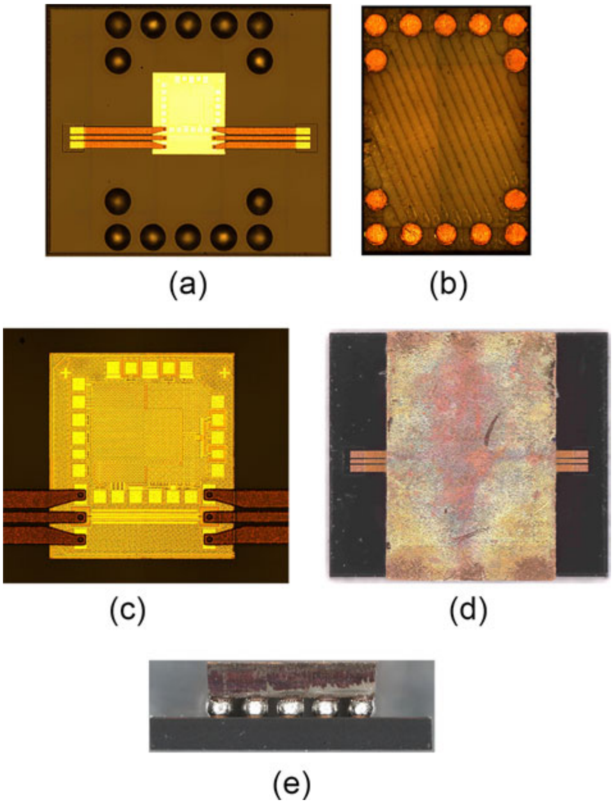


Figure 8. Chip-to-package interconnect: (a) eWLB package; (b) PCB; (c) transition and MMIC details; (d) top view of assembled package; and (e) side view of assembled package.

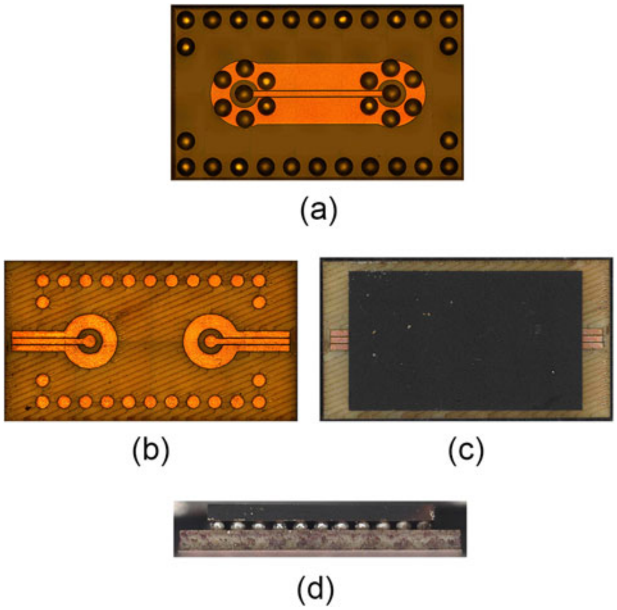


Figure 9. Package-to-PCB interconnect based on quasi-coaxial signal transition: (a) eWLB package; (b) PCB; (c) top view of assembled package; and (d) side view of assembled package.

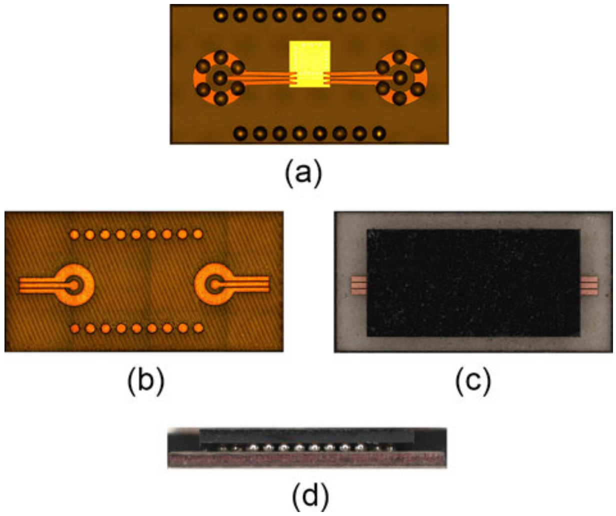


Figure 10. Complete chip-to-package-to-PCB chain with quasi-coaxial interconnect: (a) eWLB package; (b) PCB; (c) top view of assembled sample; and (d) side view of assembled sample.

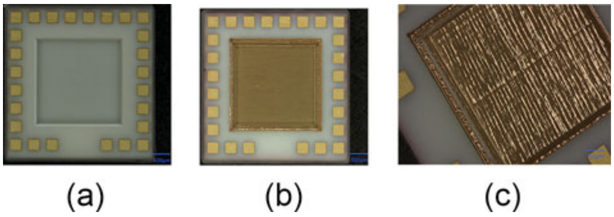


Figure 11. Manufactured prototype of horn-shaped reflector of eSRR antenna: (a) prior to metallization; (b) after metallization with AJ-printing; and (c) step with missing metallization.

9(a) and 10(a). The antenna prototype can be seen in Fig. 5(b). The fabrication and assembly of the eWLB AiP presented in this paper requires four additional key steps. The first is the structuring of the alumina substrate, the second one is re-metallizing the reflector using aerosol-jet printing, the third step is connecting the ground planes of the balun with bondwires, and the final step is the assembly of the package and the reflector. For the interconnects, the PCBs are manufactured through laser ablation as well, and subsequently soldered onto the package. The manufacturing and assembly steps are described in more detail in the following section.

Laser-structuring

The laser used in this work is the ProtoLaser R4 by LPKF – it is a green picosecond laser for cold ablation with a spot size of 20 μm. It can structure a wide range of materials including widely used PCB materials such as the gold-coated alumina or copper-plated RO4003C used in this work. For the interconnects, one side of the RO4003C substrate is structured using this laser – see Figs. 8(b), 9(b) and 10(b) for microscope photos of the PCB prototypes. As for the PCB-based reflector, a more involved process is required. A customized process is developed to manufacture the horn-shaped cavity for the antenna reflector, as the machine does not come with such a ready-to-use functionality. As a first step, a simple cavity in alumina is manufactured, and its depth measured. Knowing the depth and the number of hatching repetitions necessary to make the simple cavity allows one to determine the ablation height per repetition. In the next step, the number of repetitions per layer are chosen, so that it would cut 25 μm deep per layer, and thereafter a set of layers with decreasing cavity dimensions, is created. Controlling the difference in size between the layers means controlling the horn slope. A microscope photo of the horn-shaped cavity in the alumina can be seen in Fig. 11(a).

Aerosol-jet printing

Aerosol-jet (AJ) printing is a non-contact printing process, that can create feature sizes down to 10 μm and use a wide range of materials – including silver. The working principle is described in [28]. This work required plating the walls and bottom of the previously manufactured horn-shaped reflector. A 100 μm nozzle is the best suited for these constraints. All printing parameters are given in Table 1. The AJ5X printer by Optomec is used here, in a cleanroom environment, and 3-min oxygen plasma pretreatment was applied to the substrates. Thereafter, they were sintered for 5 min on a preheated hotplate at 250 °C. A microscopic image of the metallized horn is shown in Fig. 11(b). In order to obtain a continuous metal layer, an additional deposition step was added on the slopes. As the slope of the cavity is quite steep, some steps might not be metallized – this can be seen in the photo of Fig. 11(c).

Table 1. Aerosol jet printing parameters

Sheath	Atomizer	UA power	UA temp.
25 SCCM	13 SCCM	500 mA	24 °C
Platen temp.	Printing speed	Line width	Line pitch
25 °C	2 mm/s	28 μm	18 μm

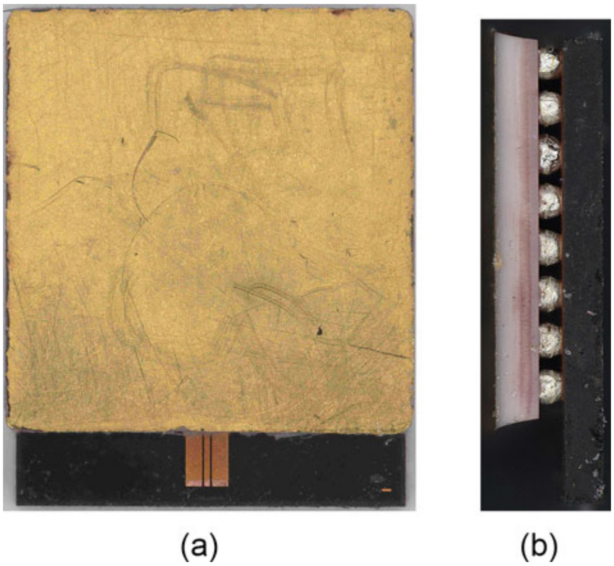


Figure 12. Microscope photo of prototype of eSRR antenna with horn-shaped reflector: (a) top view and (b) side view.

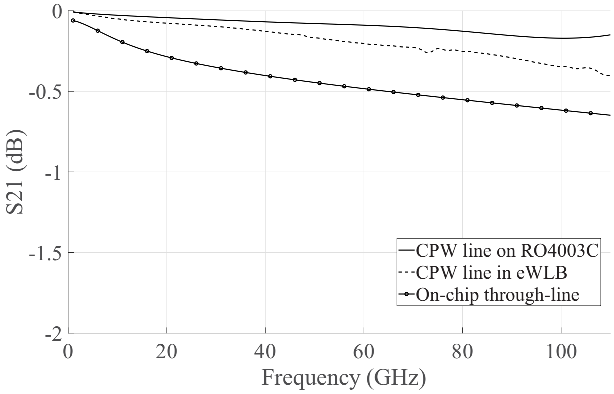


Figure 13. Simulated insertion loss of a CPW line on PCB, a CPW line in eWLB technology and the on-chip microstrip line.

Wire bonding and assembly

As mentioned above, two bond wires are added on both sides of the radial slot. An opening was left in the upper dielectric layer of the eWLB package, in the region of the balun, to expose the copper RDL layer. The dielectric opening is only 220 μm × 160 μm. The bond wires are made from gold wire with a diameter of 17.5 μm. As such it is quite challenging to fit all four, such short, bond wires in the limited dielectric opening, without accidentally shorting the signal line. A tungsten wire with a diameter of 50 μm was held in place on the signal line to prevent causing a short

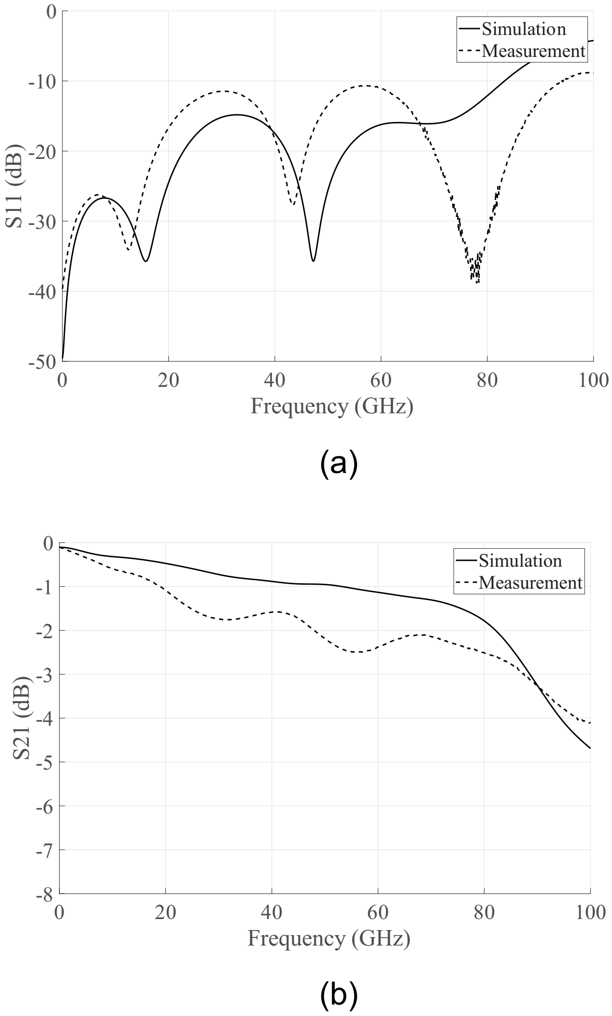


Figure 14. Measurement and simulation results of chip-to-package interconnect: (a) return loss and (b) insertion loss.

circuit with the signal line and to ensure that the final height of the bond wires were approximately 50 μm. The F&S Bondtec Series 56i wire bonder was used. The eWLB packages are manually soldered to the laser-structured PCBs, using the Finetech Fineplacer Lambda. Microscope photos of the assembled packages can be seen in Figs. 8(d, e), 9(c, d), 10(c, d), and 12.

Results

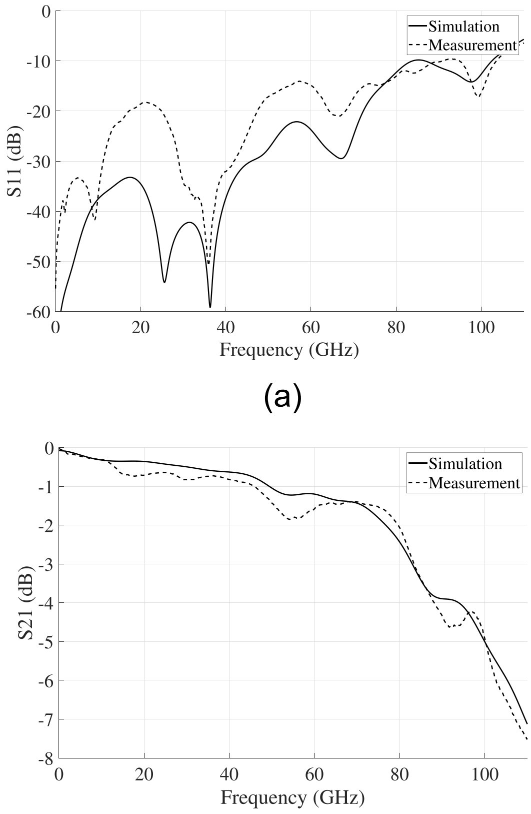
The simulation and measurement results for the interconnects are discussed first, after which the results for the high gain eSRR-based antenna are presented.

Chip-to-package-to-PCB interconnect

In this section, the results for each of the back-to-back interconnect structures are discussed. In order to calculate the loss for the interconnects or transitions, it is necessary to know the insertion loss of a 50 Ω CPW line on the RO4003C PCB substrate, a 50 Ω CPW line realized in the RDL layer of an eWLB package and that of the on-chip microstrip line. The simulation results for the insertion loss of these structures are shown Fig. 13. The CPW lines are both 1 mm in length and the on-chip through-line is 0.58 mm in length.

The simulation and measurement results of the chip-to-package interconnect, shown in Fig. 8, can be found in Fig. 14.

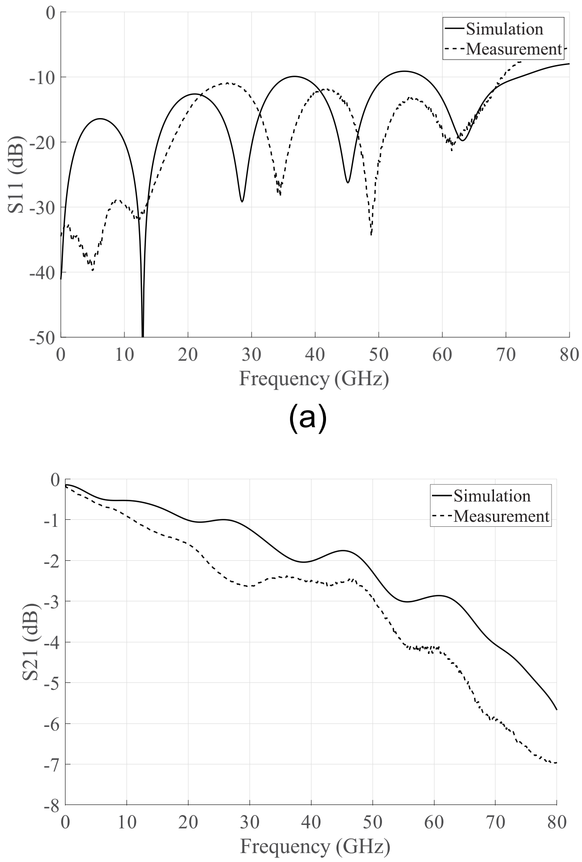
Overall, the measured and simulated results agree well. The insertion loss is less than 3 dB up to 88 GHz, for both the simulation and measurement. The return loss is greater than 10 dB up to 83 GHz, for the simulated case, and greater than 10 dB up to 94 GHz, for the measurement. The total length of the CPW line in the RDL layer of the package shown in Fig. 8, was 2.2 mm. From Fig. 13, a loss of approximately 0.17 dB/mm can be expected at 50 GHz. Therefore, 0.44 dB loss can be attributed to the CPW line in the package. Similarly, at 50 GHz, the on-chip transmission line has an insertion loss of 0.45 dB. The measured insertion loss of the back-to-back chip-to-package structure is 2.2 dB at 50 GHz – see Fig. 14. Therefore, the insertion loss per transition (including the chip pads, eWLB microvias and the taper) would be approximately 0.7 dB. The stackup of the on-chip structures manufactured in the 22 nm FDSOI CMOS technology has to be simplified, in order to simulate the detailed interconnect in a reasonable computation time. The difference between the simulation and measurement results can partly be attributed to this simplification of the on-chip structures. The differences can also stem from calibration or measurement errors, or a shift between the RDL and the chip during the overmolding process, causing a rotation or a shift in the x- or y-directions. Furthermore, the decline after 80 GHz can be due to the parasitics stemming from the overlap between the interconnect and the chip pads, as well as the parasitics of the chip pads themselves.



(a)

(b)

Figure 15. Measurement and simulation results of package-to-PCB interconnect based on quasi-coaxial signal transition: (a) return loss and (b) insertion loss.



(a)

(b)

Figure 16. Measurement and simulation results of chip-to-package-to-PCB interconnect: (a) return loss and (b) insertion loss.

The results for the back-to-back structure of the quasi-coaxial signal transition (Design A), are presented in Fig. 15. The simulation and measurement results agree very well. In both cases, the reflection coefficient is approximately equal to, or below, −10 dB, up to 103 GHz. The insertion loss of the back-to-back structure is less than or equal to 2 dB up to 80 GHz. Taking into consideration, there is 0.33 dB loss from the 2.5 mm CPW line on the PCB, and the 0.41 dB loss from the 1.65 mm long CPW line on the eWLB package (refer to Fig. 9), at 80 GHz. This results in an insertion loss of approximately 0.63 dB per quasi-coaxial transition at 80 GHz. It can similarly be determined that the loss per transition at 100 GHz is only 2.2 dB. The differences between the measurement and the simulation can be attributed to the manufacturing tolerances of the PCB substrate which is structured using laser ablation. It has been determined that the gaps between signal and ground lines of the CPW line are especially sensitive to manufacturing tolerances. Gap sizes can vary by up to ±8 μm, which can have a significant influence on the impedance of the CPW line. Due to the manual assembly, it is also possible that the BGA height, and the antenna-to-reflector distance, can vary by up to 30 μm [11]. The insertion loss of quasi-coaxial signal transition can vary by approximately 0.4 dB, for a height difference of 30 μm (at 100 GHz).

There is an increase in the radiation loss above 85 GHz. There is finite spacing between the outer solder balls that constitute the outer conductor of the coax interconnect and at low frequencies, the spacing is electrically small compared to the operating wavelength so that interconnect functions as a coaxial transmission line, supporting a quasi-TEM mode. When the frequency increases, i.e. at 85 GHz and above, the spacing between the solder balls can no longer be ignored and the TEM mode becomes distorted. This distorted mode and the accompanying increase in radiation loss, causes the sudden increase in insertion loss. The distances between the solder balls are stipulated by the eWLB design rules.

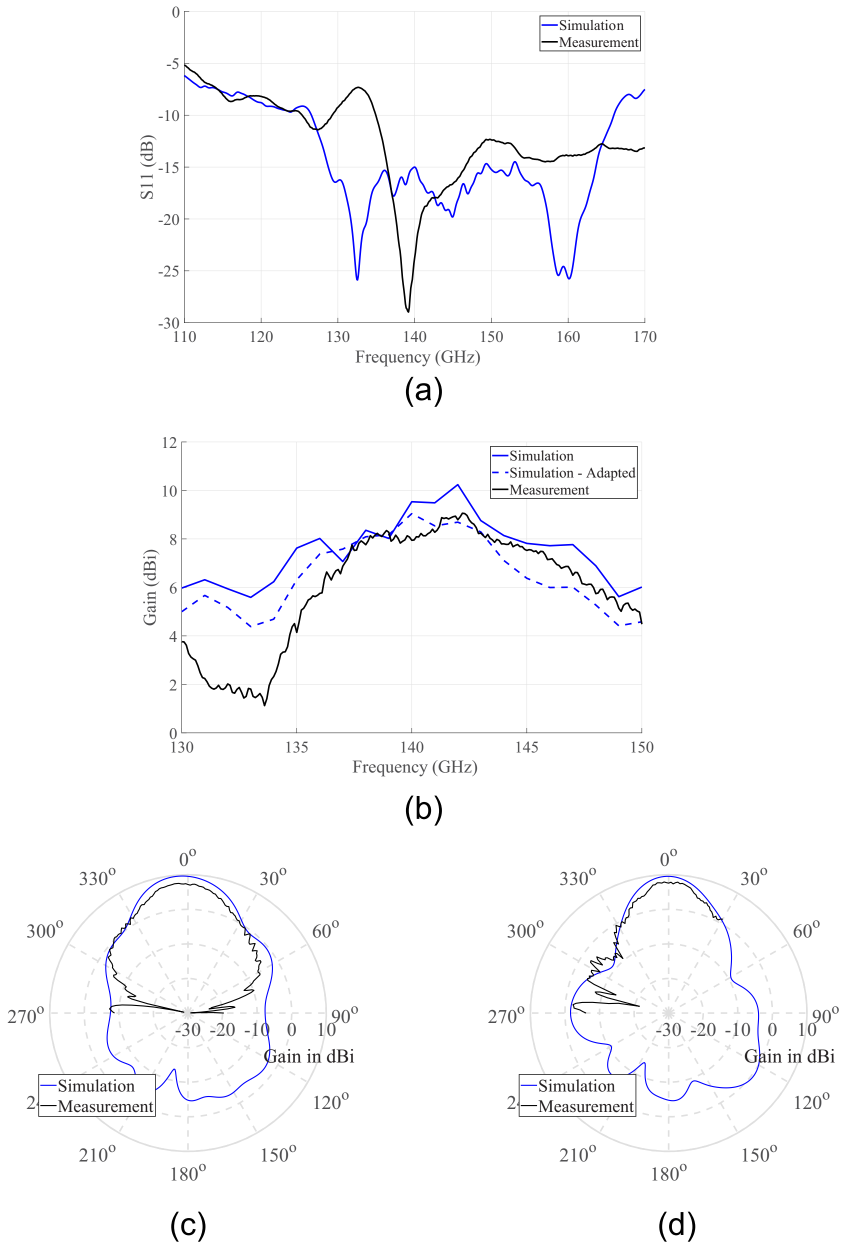


Figure 17. Measurement and simulation results of eSRR antenna: (a) reflection coefficient; (b) realized gain; (c) E-plane pattern; and (d) H-plane pattern.

A complete structure of the chip-to-package-to-PCB chain, utilizing the quasi-coaxial signal transition, is also demonstrated here. The simulation and measurement results can be seen in Fig. 16. Once more, the simulation and measurement results correspond well. The measured reflection coefficient is equal or below −10 dB up to 70 GHz. The variation in the simulation and measurement results can be attributed to the reasons discussed above.

eSRR antenna

In this section, the simulated and measured gain, far-field pattern and return loss results are presented for the differential SRR-based antenna, in Fig. 17(a–d). Figure 17(a) shows simulated and measured reflection coefficients of the eSRR antenna. The simulated reflection coefficient is below −10 dB from 126.6 to 166 GHz, while the measured reflection coefficient is less than −10 dB from 135 to 170 GHz. That results in a relative bandwidth of 26.9% and 22.9%, for simulation and measurement, respectively. The resonances in the measured reflection coefficient appear to have shifted slightly higher, by 6.4 GHz, compared to the simulated reflection coefficient. The measured reflection coefficient rises slightly above −10 dB, to −7.3 dB, from 129 to 135 GHz.

The simulated peak gain is 10.2 dBi and the measured peak gain is 9.1 dBi – refer to Fig. 17(b). Various factors contribute to the difference between the measured and simulated gain results. Firstly, it was determined that the substrate height influences the gain of the antenna. The original design assumed a substrate thickness of 508 μm, which is a standard sheet thickness. However, in reality, when measured, it was determined that the substrate was actually 480 μm in thickness. This 30 μm difference in the substrate thickness causes an overall reduction in the gain across the 130–150 GHz frequency range and a reduction of approximately 0.4 dB in the peak gain. Secondly, it is important to note that it is required to place the antenna on a Rohacell 31 HF-based supporting foam (at 26.5 GHz, $\epsilon_r \approx 1.04$ and tan$\delta \approx 0.011$) on the antenna-under-test (AUT) holder, as the direction of radiation and the probe are in opposite directions. For further details on the calibration and measurement procedures of eWLB antennas, see [11]. The Rohacell supporting foam is therefore positioned directly between the AUT and the receiver on the measurement setup. Through simulation it is determined that the Rohacell supporting foam reduces the peak gain by approximately an additional 0.8 dB. Furthermore, measurements of the bond wires after manufacturing indicated that the loop profile of the wire bonds can differ from the simulation in terms of loop height, loop profile and the tail length. The balun performance is strongly dependent on the bond wire construction [12]. As aforementioned, the BGA height, and the antenna-to-reflector distance, can vary by up to 30 μm [11] – this will in turn influence the radiation patterns; the peak gain could vary with up to approximately 0.6 dB. Several facets of the measurement procedure explained in [11] influences the measured results, such as the probe placement, the calibration procedure, the AUT alignment and the loss of the Rohacell holder at D-band frequencies. Lastly, manufacturing tolerances in the horn cavity will also have an influence on the antenna's performance. In the final manufactured prototype, the slope of the horn reflector was measured to be between 17° and 19°, and the horn depth varied between 260 and 275 μm.

The substrate height was changed to 480 μm and the Rohacell supporting foam was included in the simulation model for the eSRR antenna with the horn-shaped reflector – the simulated gain for the adapted model is also shown in Fig. 17(b). When taking these changes into account, the simulated and measured gain agrees well overall. The difference around 132 GHz can be traced back to the mismatch in the return loss around the same frequency.

The E- and H-plane radiation patterns are shown in Fig. 17(c, d). Apart for the difference in gain, as discussed earlier, the patterns agree well between measurement and simulation.

Conclusion

An SiP for a wideband digital radar, in D-band, requires broadband, high-gain antennas combined with broadband

Table 2. BGA-based quasi-coaxial interconnects

Ref.	Bandwidth (S11 ≤ -10 dB)	Insertion loss
[15]	DC – 60 GHz	3 dB @ 60 GHz
		For back-to-back hybrid model
[16]	DC – 35 GHz	0.4 dB @ 35 GHz
		For simulated transition
[17]	7–13 GHz	0.2 dB for 7–13 GHz
	(S11 $<$ −20 dB)	Measured per transition
[18]	DC – 20 GHz	5 dB @ 20 GHz
		For measured back-to-back structure
[19]	DC – 70 GHz	5 dB @ 70 GHz
		For measured back-to-back structure
[20]	DC – 97 GHz	3.4 dB @ 97 GHz
		Measured per transition
[21]	50–70 GHz	0.3 dB for 50–70 GHz
	(S11 $<$ −20 dB)	For simulated transition
This work	DC – 103 GHz	0.6 dB @ 80 GHz up to
		2.2 dB @ 100 GHz
		Measured per transition

Table 3. Summary of eWLB antennas above 100 GHz

Antenna	Frequency (GHz)	Relative bandwidth (S11 ≤ -10 dB)	Peak gain (dBi)
Single-ended			
Bow-tie slot [10]	200–300	40%	4.2
Corner-fed patch [11]	115–162	34%	6
RSRR [13]	129–159	20.8%	6.4
Differential			
Bow-tie [10]	90–140	43.5%	5.8
Bow-tie [12]	130–150	14.3%	6.3
Dipole [12]	128–158	21%	7.1
Rhombic [12]	123–170	32.1%	8.1
SSRR [14]	126–170	29.7%	8.8
eSRR (this work)	127–166	26.9%	10.2

chip-to-package and package-to-PCB interconnects. The contribution of this paper is twofold. Firstly, a wideband, low-loss quasi-coaxial signal transition is realized for the first time in eWLB technology. It was determined that the insertion loss per transition was less than 0.63 dB up to 80 GHz, and less than 2.2 dB up to 100 GHz. A chip-to-package interconnect is also demonstrated, with an on-chip microstrip transmission line in 22 nm FDSOI CMOS technology. The quasi-coaxial signal transition is combined with the chip-to-package transition to demonstrate its functionality and applicability for integration with MMICs for wide-band SiP applications in eWLB technology. In comparison with contemporary works presented in Table 2 the quasi-coaxial transition has several advantages – it is realized in commercially available technology; it exhibits very low loss up to 80 GHz; and it has the largest impedance bandwidth of the BGA-based quasi-coaxial signal transition without requiring specialized manufacturing technology.

Secondly, a modified reflector concept and a novel eSRR-based antenna were demonstrated. Prior publications of antennas realized in eWLB technology made use of a planar reflector realized on the PCB substrate. However, as the planar reflector is typically only a distance of 0.1λ from the antenna (at 140 GHz), it is inefficient in utilizing constructive interference, due the reflector, to improve the antenna gain. In the modified reflector concept, the reflector is placed approximately 0.25λ from the antenna, by micromachining a horn-shaped cavity in the alumina substrate and remetallizing the cavity through AJ-printing. The concept increases the antenna gain, with an improvement of 2.3 dB in the peak gain for the antenna with the horn-shaped reflector, in comparison with the antenna with the planar reflector. A significant improvement is especially noticeable at the higher frequencies – an improvement of up to 5.3 dB can be seen around 149 GHz. The simulated peak gain is 10.2 dBi and the measured peak gain is 9.1 dBi. Table 3 compares antennas realized in eWLB technology for frequencies above 100 GHz in order of ascending peak gain. The AiP with the horn-shaped reflector presented here, surpasses [14] as the single antenna element with the highest gain, in eWLB technology, above 100 GHz.

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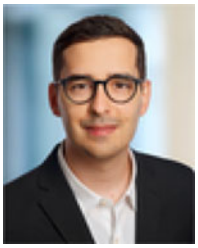

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