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Automated Sample Preparation of Low-k Dielectrics for FESEM

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Rapid, efficient and automated sample preparation of microelectronic materials containing high-k dielectrics has been recently demonstrated.[1] A standard process cycle combines plasma cleaning (PC), argon ion beam etching (IBE), reactive ion etching (RIE), and ion beam sputter coating (IBSC) in a single vacuum chamber. An additional plasma cleaning step can be inserted after the RIE step, so that any residual contamination is removed prior to imaging or final sputter coating. This technique has now been extended to microelectronic materials that contain low-k dielectrics.

Because of their complex chemistry and low average atomic number, cross sections containing such layers often become damaged when mechanically sectioned or polished. The microstructure of an IMEC# Cu/porous-SiLK™ dielectric resin single damascene wafer after cleaving and plasma cleaning is shown in Figure 1. The Cu lines separated by the porous SiLK Y resin are barely visible below the rough fracture surface of the Si oxide and nitride layers. This sample was then processed according to the protocol summarized in Table 1. The total processing time was 28.5 minutes.

RIE of the high-k and low-k dielectrics was accomplished by forming a reactive gas plasma of Ar, CF_4 and CHF_3 which was directed perpendicular to the sample surface. Although chemically inert, the energetic Ar ions act to break Si-Si bonds, supplying Si to stabilize SiF_4 vapor formation. Once the CF_4 is ionized to CF_3, F is released (CF_4 + e- ➔ CF_3 + F + e-). This F absorbs and etches Si to SiF_4 (Si (s) + 4F ➔ SiF_4 (vapor). CHF_3 is added as a F "deficient" species to enhance the etch selectivity of SiOx with respect to Si. Depending on the local gas dynamics and rate of reaction, products of the reaction may not volatize, but remain at the sample surface. [2] Plasma cleaning with Ar/25%O_2 has been useful in removing this residue, which is a complex fluorocarbon polymer.

After FESEM imaging to assess the uncoated sample surface, a conductive coating of 6nm of Cr was added in a stand-alone sputter coater. This surface was re-imaged at 10kV and 100kX, Fig. 2. The action of Ar ions during IBE and later RIE resulted in the decoration of the Cu lines. The Ar/CF_4/CHF_3 RIE resulted in delineation of the Si nitride and oxide, as well as of the porous SiLK resin. No significant amount of RIE residue was detected.

References

[1] R.R. Cerchiara, P.E. Fischione, J.J. Gronsky, W.F. Hein, D.D. Martin, J.M. Matesa, A.C. Robins and D.W. Smith, "Recent Developments in Automated Sample Preparation for FESEM", Proceedings of the 29th International Symposium for Testing and Failure Analysis, Santa Clara, CA, Nov. 2-6, 2003, pp. 288 – 300.
[2] S.M. Rossnagel, Handbook of Plasma Processing, Noyes Publications, New York, 1990.

Sample courtesy of the Inter-University Microelectronics Center (IMEC), Belgium
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TABLE 1: Sample Preparation Protocol for IMEC Cu/P-SiLK™ Single Damascene Wafer

Step	Process Gas	Time (min.)	Result
PC	Ar/25%O_2	5	Removal of Hydrocarbon Contamination
IBE	Ar	20	Planarization
RIE	Ar/35%CF_4/30%CHF_3	1.5	Selective Etching of Low-k
PC	Ar/25%O_2	2	Removal of Residue from RIE

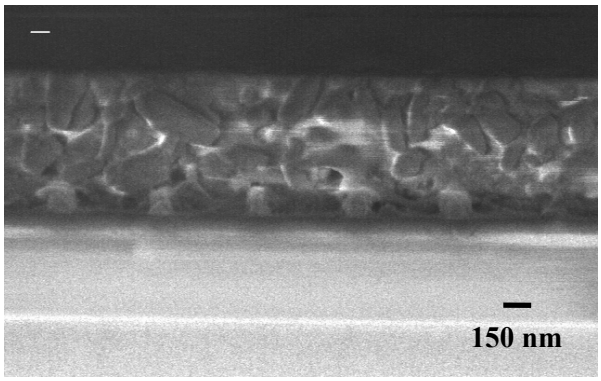

FIG 1: IMEC Cu/P-SiLK™ single damascene wafer after cleaving and plasma cleaning

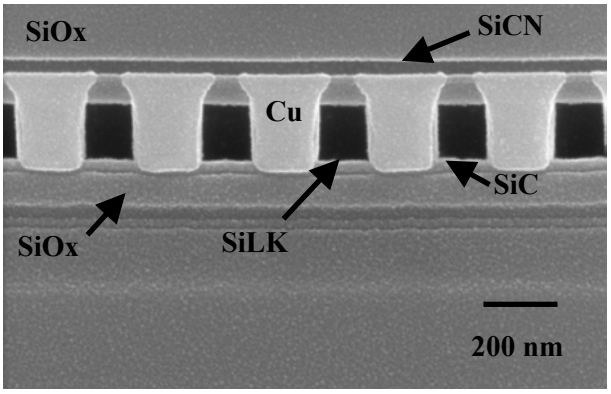

FIG 1: Surface of cross section after PC + IBE + RIE +PC, followed by coating with 6 nm Cr

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