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An Effective Approach to Extract Cross-Sectional Information from Top-Down SEM for 20nm & 14nm Transistor Nodes in Semiconductor Wafer-Foundries

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With continuous shrinkage of semiconductor transistor nodes, physical failure analysis (PFA) heavily relies on transmission electron microscopy (TEM) to conclusively identify root-causes of yield detractors [1~4]. Due to the time-consuming process and challenges in preparing TEM lamella, it is critical to develop effective alternatives to reduce the TEM workloads and therefore to efficiently shorten turnaround time, while still being able to discern defects / failure modes. Full utilization of various scanning electron microscopy (SEM) modes from top-down view to extract / estimate cross-sectional information below the sample surface is one of multiple initiatives to accomplish this goal.

Fundamentally, the major contributor to the huge difference in the imaging quality of SEM versus TEM is the existence of an energy-activated zone (EAZ, so-called “tear-drop / pear-shaped” zone) underneath the surface in the bulk sample by SEM (“reflective” imaging mode) versus the true transmission mode in TEM on thin lamella samples. Thus, the true resolution of SEM is not dictated purely by the acceleration voltage, but a “resultant resolution” governed by the size of EAZ which is caused by “extra” electron signals coming from the EAZ back to detectors (rather than only from the desired point of incident beam at the sample surface). This is why SEM images are usually inevitably blurry; compared to TEM images which are always superiorly sharp and have better contrast (e.g., due to diffraction contrast). In practice, the best way to improve the “resultant resolution” of SEM is to reduce EAZ by lowering the acceleration voltage (e.g., from 30kV to 1kV or even below), as long as sufficient signal to noise level is maintained. The penetration depth of the EAZ varies from hundreds to dozens of nanometers, depending on the material and the voltage applied to generate the electron beam in the SEM.

However, in the real world of PFA at wafer-foundry, where timely root-cause identification and analysis is a virtue, this “ADVERSE effect” in SEM mode with “extra signals” from various depth beneath the sample surface can prove to be useful if applied for appropriated purposes / features of interests, sometimes even without further needs to scrutinize defects by TEM cross-section. As the size of the electron beam and sample interaction zone in SEM mode can be controlled by adjusting SEM parameters, (e.g., the accelerating voltage ranging from 0.5kV to 30kV), it is possible to SELECTIVELY reveal key features of interests across various penetration depth below the SEM sample surface before cross-sectional TEM. Examples illustrated here demonstrate such effectiveness by utilizing various top-down view SEM imaging mechanisms, e.g., low-kV passive voltage contrast (PVC), high-kV secondary electron (SE) imaging and back scattered electron (BSE) imaging with a combination of variations in SEM beam energy. Figure 1 is an illustration of a cross-sectional view of important contact levels adjacent to 20nm or 14nm SRAM transistor - PC gate (traditionally named after poly-Si conductor), such as contact to active area (CA) and contact to PC gate (CB). The integrity of these key features determines if transistors function properly or not, and thus directly links to the yield

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productivity. It is worth mentioning that each contact level is at dozens of nanometers beneath the sample surface. This enables selective detection of features at various depth levels by adjusting the EAZ. Figure-2a is a PVC image with 1kV where only very shallow region near top surface of CA/CB layer (Depth-A in Fig-1) selectively highlighted. The wafer was delayered till top of CA/CB layers. By adjusting the acceleration voltage of SEM beam and using different SEM imaging signals, features of interest at various depth levels can be easily delineated, unless severe abnormality observed, there is no need to do additional cross-sectional TEM or additional delayering. Figures 2b & 2c are SE and BSE SEM images corresponding to deeper region within the surface that reveal both CA/CB and PC level, as illustrated in Depth-B in Fig-1. When appropriately applied to selectively reveal various layers beneath sample surface, SEM top-down view provides a quick means to screen the sample in order to pin-point real defects of interest that can significantly reduce TEM imaging in wafer-foundry.

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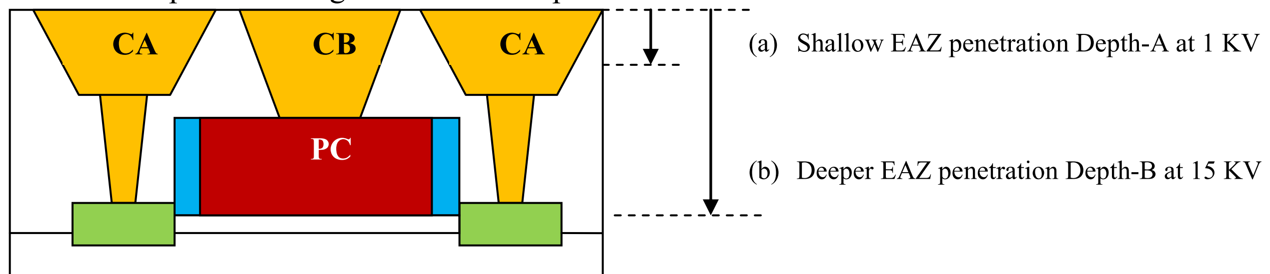

Figure 1. An illustration of cross-sectional view of a SRAM transistor stack; and variations of SEM penetration depth, (a) at a low-kV for PVC image; and (b) at a high-kV for SE and BSE images.

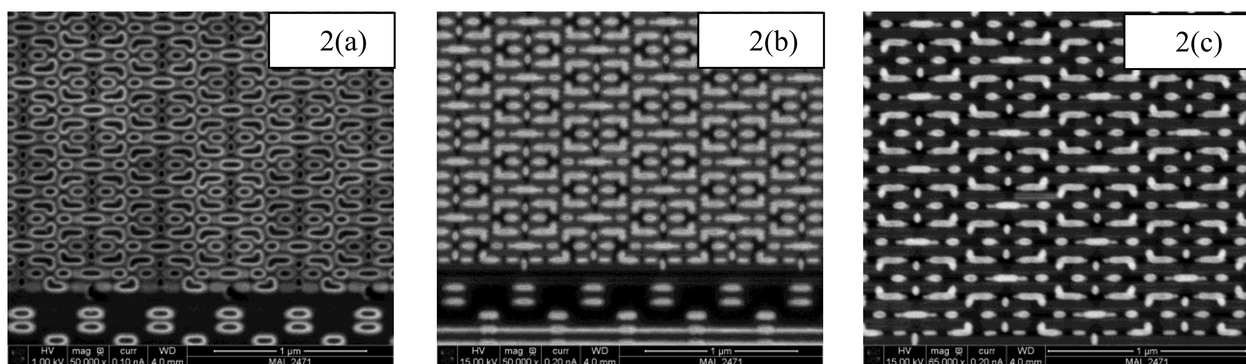

Figure 2. (a) PVC at 1kV revealed features at CA/CB depth level; At 15kV, both CA/CB and PC gate depth level clearly delineated, as shown in (b) SE image, and (c) BSE image.

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