

In Situ Nanoprobng Tools for Fault Localization and Defect Characterization

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As the semiconductor devices that power our modern world continue to shrink, more and more of the research & development process is moving into Scanning Electron Microscope (SEM) and Focussed Ion Beam (FIB) tools. The SEM is most commonly used for visualizing the devices under test, however there are a number of additional ways to employ the electron beam for fault localization and failure analysis.

Characterizing transistors is one of the most common tasks for in situ nanoprobng. This is usually achieved by landing a number of probes - typically three or four - on the sample surface and bringing them into contact with the corresponding sites on the sample for the transistor's source, gate, and drain. Subsequently various measurement recipes are available to the investigator in order to document the transistor's performance.

The difficulty in performing the steps described above scales with the size of the structures being investigated. In order to successfully record data from structures that are in the nanometer scale (such as semiconducting nanowires or lithography structures), it is necessary to have probe tips with appropriate tip radii as well as a means of gently placing these probe tips on the sample surface at the desired location. At the nanometer scale, thermal drift can be a significant factor that needs to be considered.

While performing nanoprobng experiments, it is very important to differentiate between physical contact between the probe tip and the substrate (contact pad, nanowire, carbon nano tube, etc.) and electrical contact between the probe tip and the device under test. Physical contact is achieved by approaching the sample surface with a probe tip mounted to a micro- or nanomanipulator. Micromanipulators are typically driven by piezo motors allowing for precise control over the probe tips' positions. Depending on the structure size that the measurements are to be performed on and, correspondingly, the probe tips' radii, This step can be more or less difficult. However, using the SEM image, physical contact can be reliably confirmed.

A number of factors may prevent a probe tip that is in physical contact with the sample surface to also be in electrical contact with the sample. These include thin oxide layers that are invisible to the electron beam or carbon contamination layers deposited by the electron beam, among others. In order to quickly assess whether a given probe tip is in good electrical contact with the sample, a contact testing tool is introduced. This tool applies repeating voltage ramps to the individual probe tips and records the current responses. This task is performed ten times per second and the results are displayed in real-time - thus the experimenter is provided with instant feedback on each tip's contact status.

Beyond nanoprobng, there are various methods that can be used to home in on the area within the sample that requires closer investigation. A number of these methods will be presented in this work. One such method is Electron Beam Induced Current (EBIC).

EBIC images are created from electrons that penetrate through the semiconductor's oxide and metal layers to the p-n junction. The electron hole-pairs that are generated in this process are separated by the diffusion voltage and measured as a current that flows through the micromanipulator's probe tip. The current signal is converted to a voltage and fed back to the SEM in order to obtain an image of current flow within the sample. Light and dark areas in the image indicate p-n junctions (n- and p-wells to the substrate). Grey regions indicate areas where no current is flowing. This method is widely employed in semiconductor R&D but also in various fields of research including other semiconducting nanostructures such as novel solar cell designs. [1, 2]

Another method for locating the precise region of interest is Current Imaging. In this technique, a needle is brought into contact with the sample and scanned over the surface while applying a bias to the needle or the sample and using the sample bulk or another needle to read the sample's current response at each point of the scan. In this way a map of current flow within the scanned area can be generated. [3]

References:

[1] R. Ring *et al*, ISTFA 2015: Proceedings from the 41st International Symposium for Testing and Failure Analysis

[2] J Ledig, X Wang, S Fündling, H Schuhmann, M Seibt, U Jahn, H Wehmann, and A Waag, *Phys. Status Solidi A*, 1-8 (2015), p. 1-8

[3] M Kemmler, A Rummel, K Schock, S Kleindiek, 2015 IEEE 22nd International Symposium on the Journal Physical and Failure Analysis of Integrated Circuits (IPFA)

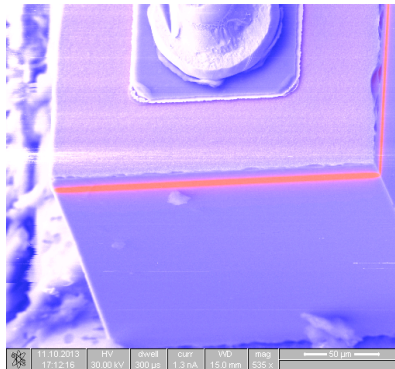


Figure 1. Colorized overlay of SEM image and EBIC result showing the p-n junction in an LED.

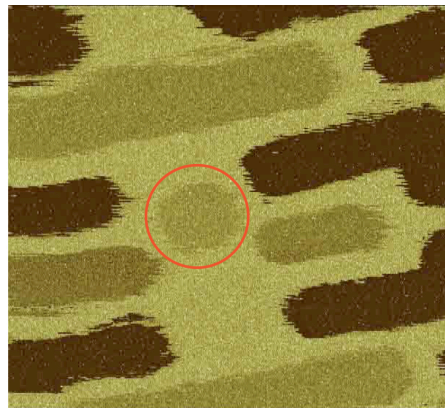


Figure 2. Current response map on a 22 nm SRAM device. The red circle marks the location of a leaky gate.