

## Utilizing Scanning Probe Microscopy to Investigate Preferential Conductive Paths through Polycrystalline BaTiO<sub>3</sub> Dielectric Layer of MLCCs

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Multilayer ceramic capacitors (MLCCs) with barium titanate (BaTiO<sub>3</sub>) dielectric and nickel (Ni) base-metal electrodes (BMEs) are ubiquitous passive components in modern microelectronics in which reliability is limited by resistance degradation [1]. Identification of structural features responsible for charge transport through dielectric layers is critical for the understanding and improvement of device performance and reliability. Microstructure has been correlated to current leakage in a number of different metal oxide dielectrics by conducting mode Scanning Probe Microscopy (SPM) techniques [2-4]. In certain polycrystalline materials, in particular, in HfO<sub>2</sub>, grain boundaries were shown to control charge conduction, which proceeds via oxygen vacancies accumulating along the grain boundaries [3]. In this study, we investigate relative contributions of grains and grain boundaries to the leakage current through polycrystalline BaTiO<sub>3</sub> films using Conductive AFM (C-AFM) with a Bruker Dimension-Icon AFM using the PeakForce Tapping mode.

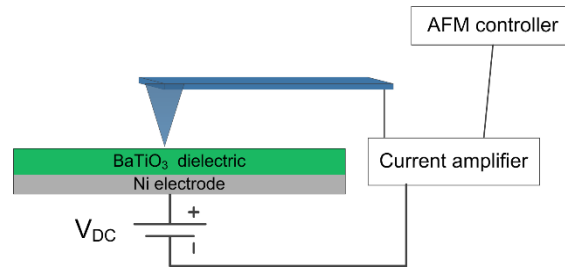
C-AFM measurements were performed by scanning a conductive doped-diamond coated silicon cantilever over the surface of a dielectric layer of a commercially available BME-MLCC. The dielectric layer was exposed by removing the top electrode, DC bias was applied to the bottom electrode as shown in Figure 1. Simultaneously acquired topography and current maps, as shown in Figure 2, demonstrated higher conductance at grain boundaries compared to bulk grains. In Figure 2e, currents measured across a particular grain boundary (shown in Figure 2 a-c, by the dashed lines with colors coordinated to the plots in Figure 2e) are shown to increase with bias voltage. The magnitude of leakage current through grain boundaries varied, possibly due to variations in grain boundary composition and microstructure. Current-voltage (I-V) plots were measured by sweeping the DC voltage from 0 to 10 V at a given site grain boundary and bulk grain (GB and G in Figures 2 a-d) by keeping the tip at fixed location in contact with the surface. The difference in current values measured through grain and grain boundary sites became more pronounced at higher voltages (Figure 2f).

Our C-AFM results indicate higher current through grain boundaries compared to bulk grains in the polycrystalline BaTiO<sub>3</sub> dielectric layer. Leakage current along grain boundaries was found to increase under higher applied DC voltages indicating that the current was controlled by a field-activated carrier transport.

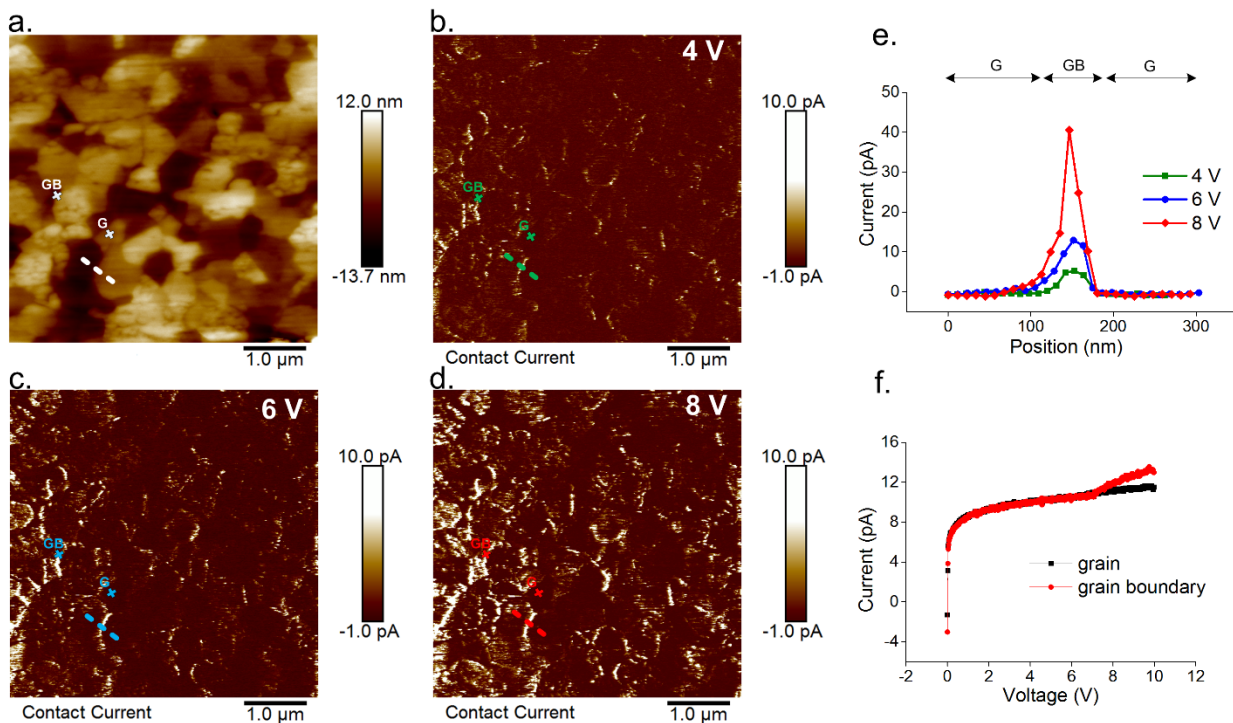
The conventional belief is that leakage current passes preferentially through BaTiO<sub>3</sub> grains while grain boundaries play the role of Schottky barriers suppressing leakage that is affected by oxygen vacancies. Our data indicate, on the contrary, that grain boundaries are the preferential path of leakage currents. We are investigating the role of grain size, dopants, and processing conditions (such as reductive or oxidative anneals) in controlling stress induced leakage in these types of materials.

## References:

- [1] H Kishi, Y Mizuno and H Chazono, *Japanese Journal of Applied Physics*, **42** (2003), p. 1.  
 [2] SM Gheno *et al*, *Journal of American Ceramic Society*, **91** (2008) p. 3593.  
 [3] G. Bersuker *et al*, *Solid-State Electronics* **65–66** (2011) p. 146.  
 [4] S Hong, in “Nanoscale Phenomena in Ferroelectric Thin Films” (Springer Science & Business Media, New York), p. 219.



**Figure 1.** Schematic diagram of C-AFM measurement experimental set up.



**Figure 2.** C-AFM measurement result. (a) Topography image (b-d) Current maps at 4 V (b), 6 V (c) and 8V (d) of the polycrystalline BaTiO<sub>3</sub> dielectric layer of a MLCC, brighter colors in current maps represent higher current values. (e) Current profiles across a grain boundary region as marked by colored dashed lines in the current maps (b-d) at various DC voltages. (f) Current vs Voltage curves measured on grain boundary (GB) and grain (G) sites.