

## TEM Sample Preparation for the Semiconductor Industry - Part 2

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In the November issue of this publication, we described how focused ion beam (FIB) microsurgery is used to successfully cross-section and prepare material-specific samples for SEM and TEM analysis. Material specific samples have two or more components possessing different characteristics, such as hardness and chemical etch or sputtering rates. Traditional sample preparation techniques (mechanical grinding and polishing, broad ion beam etching, and chemical etching) alter, delaminate, or destroy these samples.

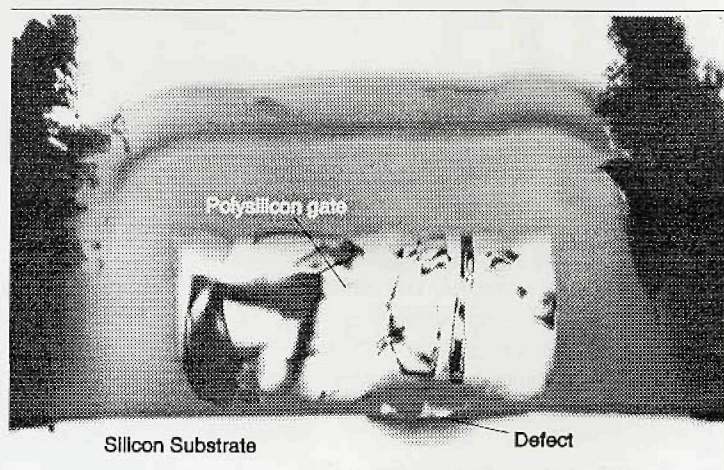
FIB handles the preparation of these difficult samples well because of its milling geometry and the high current density of the small beam.

In Part 2 of this series, we detail how FIB is also the tool of choice to prepare *site-specific samples*, particularly for transmission electron microscopy (TEM) analysis.

A site-specific sample has a particular (and sometimes unique) feature of interest that is very small (typically submicron). While this feature is located within a known volume of the sample, its *exact* location may be unknown. TEM analysis of process features and defects in the semiconductor manufacturing environment almost always requires the thin sectioning of these challenging site-specific samples. One example follows:

### Investigating an Electrical Test Failure

In this example, our customer had a chip that failed initial electrical test. After additional electrical leakage tests, the design engineers were able to reduce their vector set to pinpoint the problem to a specific field effect transistor (FET). The cause was thought to be a very small (0.1 micron) break in the FET's gate oxide. The gate is a square of polycrystalline silicon approximately 1  $\mu\text{m}$  by 1  $\mu\text{m}$  located on top of a silicon dioxide barrier layer that is 17 nm thick. This problem was affecting



The TEM image of the thinned site-specific sample clearly shows the structure of the gate region, including the defect. The defect was created from a voltage breakdown of the gate structure, which locally heated the defect region, creating an amorphous silicon region.

the manufacturer's yield, so it was very important to completely diagnose the problem and eliminate the cause. Conventional grinding and broad ion beam polishing could not be used to prepare this sample because the defect's exact location could not be determined from examining the surface with either an optical microscope or an SEM.

Using the device's design layout, the area surrounding the questionable FET was optically identified and mechanically removed. The sample was cut to 3 mm in length and mounted to a modified TEM grid that facilitated FIB milling. The sample was mechanically ground to a thickness of approximately 70 microns and loaded into the FIB 200 using FEI's TEM sample vise.

Four FIB images showing the progress of the sample preparation are presented to the right. Surface features visible in the FIB image provided the reference to locate the buried transistor and define the large trench mill patterns. The large trenches were milled using a 7 nA probe current for rapid material removal rates (top left). Subsequent thin slices were then milled out in 50 nm steps. After each thin slice was removed, the cross-section was imaged using a very low FIB current to both minimize sample damage and provide the highest spatial resolution.

After several slices were removed, the components of the transistor were identified (bottom left). After the 12th slice, the FIB image revealed a break in the transistor gate (top right) despite the low ion dose (< 1 pA) used for imaging. The back side of the sample was then quickly milled until the film was <100 nm thick and electron transparent (bottom right). No sample tilting was required to obtain parallel membrane walls because of the beam shape provided by FEI's Clean Cut Optics™. After milling, the sample and grid were transferred to the TEM.

The TEM image above clearly shows the structure of the gate region, including the defect. Diffraction analysis identified the substrate as single-crystal silicon, the gate as polycrystalline silicon, and the oxide barrier as silicon dioxide. The defect occurred after the gate voltage was great enough to break down the gate oxide. High current was then able to flow through this localized break heating the region to the melting point of silicon. Fast cooling then froze the silicon in an amorphous state.

It would be very difficult (if not impossible), much more time consuming, and extremely laborious to prepare the sample described above with any technique except FIB. The FIB's advantage is its ability to both place the final membrane with an accuracy of 0.1 microns and produce images with spatial resolution better than 10 nm. All other techniques would require the user to employ at least two tools - a broad-beam ion mill and an SEM - and would not provide the real-time control that the FIB provides.

We appreciate the permission of our user to share this example with the readers. ■

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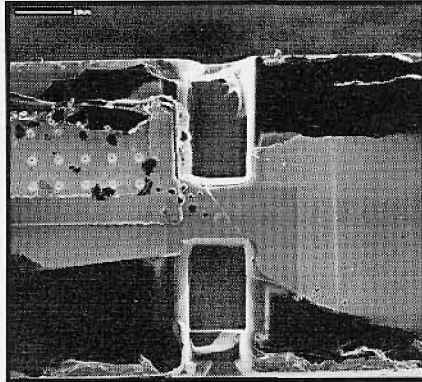
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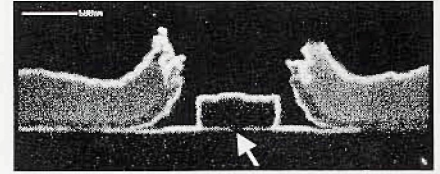
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These FIB images were acquired during the preparation of a site-specific sample for TEM analysis. The challenge was to find a defect causing electrical failure in a specific field effect transistor and prepare a TEM film containing this defect.

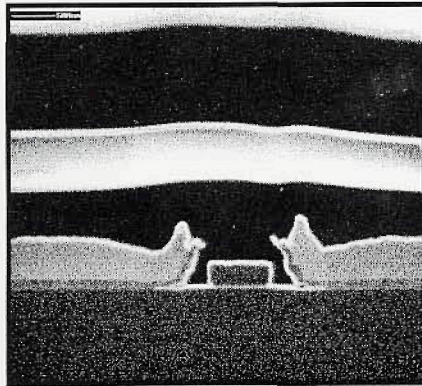
● Initial large trenches were rapidly milled using a 7 nA beam current



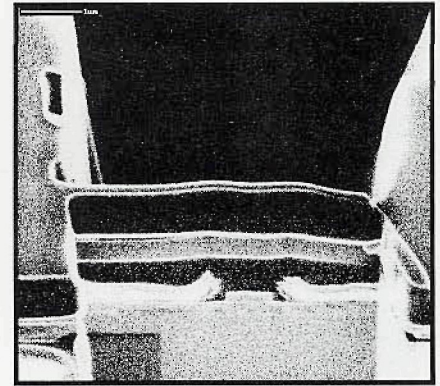
● After the 12th slice, the defect was seen as a break in the transistor gate.



● After a series of thin slices were removed, the transistor components were revealed, but the defect was not yet visible.



● After locating the defect, the back side of the film was milled to be electron transparent (thickness <100 nm). So sample tilt was required to obtain parallel membrane walls because of the beam shape provided by FEI's Clean Cut Optics.



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