DOI: 10.1017/S1431927605504458
Microsc Microanal 11(Suppl 2), 2005

HAADF Imaging and Low-Loss EELS Investigation of HfO_2/TiN Interfaces in High-*k* Gate Stacks

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Continued scaling of feature sizes in complementary metal-oxide-semiconductor (CMOS) has resulted in a need to replace SiO_2 and polycrystalline Si as gate dielectric and gate electrode, respectively. HfO_2 dielectrics and TiN metal gate electrodes have been the subject of extensive studies [1-6]. One of the requirements for a gate dielectric is its thermal stability in contact with Si and the gate electrode up to 1000°C, which is necessary in CMOS processing. Stoichiometric HfO_2 is stable in contact with Si [7], however films deposited for this application can be oxygen-rich or oxygen-deficient depending upon growth conditions. Non-stoichiometric films show reactions not predicted by equilibrium phase diagrams. We have investigated the interfaces in HfO_2/TiN stacks using high-angle annular dark-field (HAADF) imaging and electron energy-loss spectroscopy (EELS) in scanning transmission electron microscopy (STEM).

HfO_2 dielectrics were grown by atomic layer deposition on Si substrates followed by a post-deposition anneal in O_2 at 700°C for 60 seconds. Gate stacks were formed by depositing 20 nm TiN by ALD followed with 20 nm TiN grown by DC sputtering. This sample is referred to as as-deposited. Another set of stacks were exposed to rapid thermal anneals in N_2 ambient at 700°C, 800°C, and 900°C, respectively. TEM samples were prepared by standard sample preparation techniques and a final low energy ion milling step. In addition, a reference sample for EELS was made from commercial powder HfO_2. HAADF imaging and EELS were performed using a 2-3Å probe in a field-emission TEM operated at 300 kV.

Fig. 1 shows the HAADF images of the (a) as-deposited and (b) 900°C stacks for comparison. HAADF images show that the HfO_2 is polycrystalline in all samples. All samples showed a thin interfacial SiO_2-like layer at the Si interface. No difference in interfacial roughness is detected at the Si interface of the as-deposited stack and the stacks annealed up to 800°C, whereas roughening at the TiN interface is observed with increasing anneal temperatures. In the 900°C stack, roughening is observed at both Si and TiN interfaces. The severe roughening at the top interface is reflected as an overlap of the HfO_2 and the TiN grains. Low-loss EELS confirm this interfacial roughness. Ti $L_{2,3}$- and O K-edge EELS did not indicate the presence of an interfacial reaction layer such as TiO_2.

Fig. 2 shows the low-loss EELS recorded from the middle of the HfO_2 films (~13 nm) and from the HfO_2 reference powder. The low-loss spectrum more closely resembles that of the reference HfO_2 at higher anneal temperatures. An increase in intensity at the band edge for the 800°C and 900°C films is detected; however it is not sharp and begins before 5.6 eV. This could indicate defect states within the band gap. A sharp rise in intensity is not seen at the band edge for the 700°C and the as-deposited films. Peak B has the largest intensity in the reference HfO_2 and is assigned to an interband transition from the highest occupied valence O 2p state to the lowest unoccupied Hf 5d state in the conduction band. This peak appears as a shoulder in the as-deposited sample and transforms to a peak with annealing. The peaks at higher energies are assigned to the HfO_2 $O_{2,3}$-edges [8]. Peaks narrow with increasing anneal temperatures.

In summary, HAADF imaging and EELS show that changes within a crystalline HfO_2 film still occur with annealing. Interfacial roughening increases with anneal temperature. However, increasing the temperature causes the electronic structure to resemble that of bulk HfO_2 [9].

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[9] This research was supported by SRC. M.P.A. also acknowledges the scholarship provided by Intel/SRCEA.

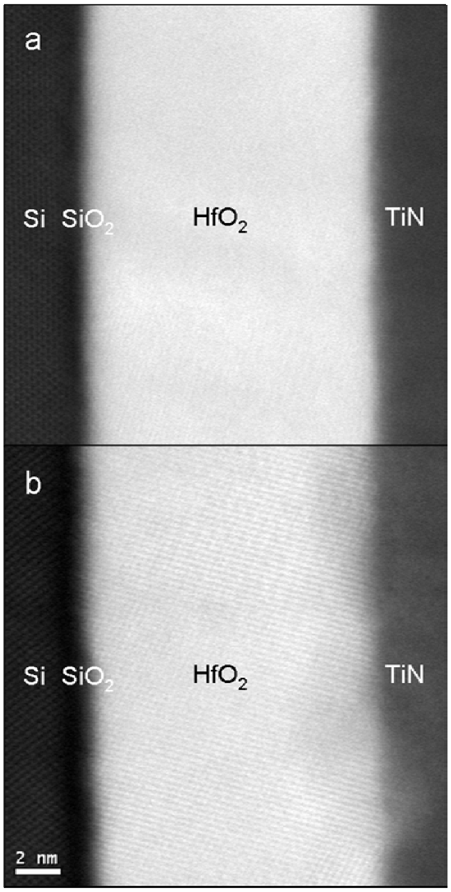

Fig. 1. HAADF images of (a) as-deposited and (b) 900°C gate stack. Note interfacial roughening.

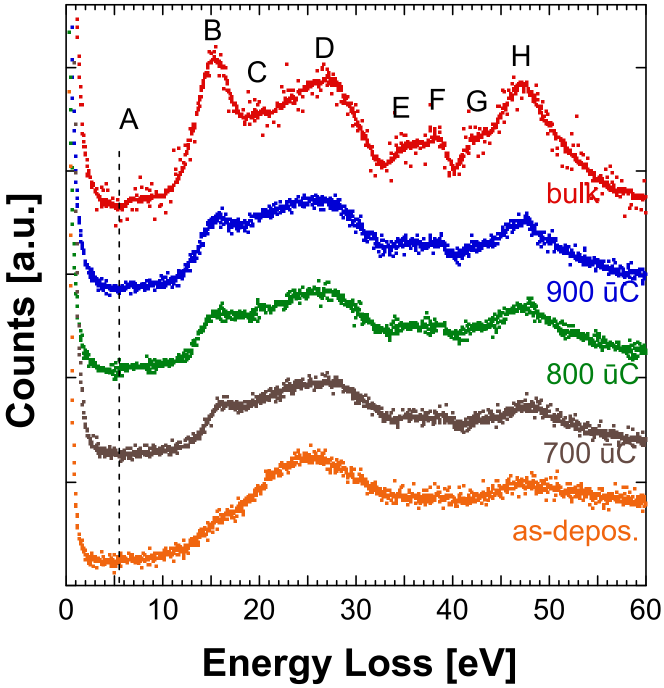

Fig. 2. Low-loss EELS recorded from middle of HfO_2 films and reference powder.