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Performance of hydrogenated diamond MISFET using Zr-Si-N as the dielectric layer

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ABSTRACT

To better stabilize the hydrogen-terminated surface, a diamond based metal-insulator-semiconductor field-effect transistor with Zr-Si-N dielectric layer has been investigated. On the diamond epitaxial layer grown by microwave plasma chemical vapor deposition system, Pd films were patterned as the source and drain electrodes by photolithography and electron beam evaporation methods. Then, a Zr-Si-N dielectric layer and W metal film were fabricated as the gate structure by radio frequency magnetron sputtering technique. The device illustrates p-type depletion mode, in which the threshold voltage, maximum transconductance, drain current maximum, capacitance and dielectric constant were calculated to be 3.0V, 1.27mS/mm, -5.16 mA/mm, 0.275μF/cm^2 and 7.8, respectively. The result suggest that Zr-Si-N dielectric layer is shown to have the ability to protect the two-dimensional hole gas.

INTRODUCTION

Diamond film collects many outstanding properties due to its wide band gap energy(5.5eV), high break-down field(>10MV/cm), large carrier saturation velocity(1.5×10^7cm/s), large thermal conductivity((22 W/K.cm), high carrier mobility(3800–4500cm^2/V.s), making it have potential applications in the fields of high power and high frequency electron devices[1-4]. Although undoped diamond is highly insulating, the hydrogen-terminated diamond surface exhibits p-type conductivity without impurity doping, with sheet hole density and hole mobility of 10^{13} cm^{-2} and 50–150 cm^2/V.s, respectively [5,6]. The two-dimensional hole gas of hydrogen-terminated (H-terminated) diamond which provides p-type surface conduction without doping impurities has been widely investigated [7,8]. Moreover, high-frequency, high-power FETs employing such a p-type conductive channel can operate at millimeter-wave frequencies with cut-off frequency f_T of 45 GHz and f_{max} of 120GHz [9] and RF output power density of 2.1W/mm at 1GHz [10]. Nevertheless, the two-dimensional hole gas (2DHG) is vulnerable to the ambient environment because of factors such as chemical reaction and heat [11]. Oxidation of diamond surface may result in the loss of 2DHG, then the performance of FET device may decline. Stabilization of the surface conduction channel is still a key issue. Dielectric layers SiO_2, Al_2O_3, AlN, for instance, have been deposited on H-terminated surface to protect the conduction channel for stabilizing the adsorbates [12-15]. Metal-nitride alloys such as ZrN and Si_3N_4, have been used for anti-diffusion of oxygen, and the Zr-Si-N which consists of ZrN and Si_3N_4, whereas, performed better oxidation resistance[16-18]. Since Zr-Si-N contains no oxygen, the hydrogen-terminated diamond surface could be passivated without being oxidized, resulting in stabilization of the 2DHG. However, few articles reported diamond based field-effect transistors with Zr-Si-N dielectric layers.

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In this study, a diamond metal insulator semiconductor field effect transistor (MISFET) based on a p-type surface conductive layer with a Zr-Si-N dielectric layer was fabricated, and its properties were studied.

EXPERIMENT

High-quality homoepitaxial films were grown on a [100]-oriented Ⅱa CVD single-crystal diamond substrate (CVD synthesized) with dimension of $3\times3\times0.5mm^3$ in a 1.5 KW AsteX 5200 reactor. At first, the single crystal diamond was treated with alkali and hot-acid to clean non-diamond phase and metal ions. Then, the substrate was loaded into the Microwave Plasma Chemical Vapor Deposition chamber for electronic grade diamond epitaxial. The total-flow rate was 500 sccm during the growth, with 1% CH_4 diluted in purified H_2. The substrate temperature, the microwave power, and the process pressure were 900℃, 1kW and 100Torr, respectively. After growth, the samples were kept in H-plasma for 10 min and then cooled down to generate the 2DHG channel.

To acquire the quality of single crystal diamond, the X-ray diffraction scattering and Raman measurements had been carried out. For better adhesion and low specific resistance, Pd was directly deposited by electron beam evaporation on the H-terminated diamond surface as drain and source electrodes [19]. After this, Zr-Si-N layer of 25nm in thickness was deposited as the insulator layer by sputtering technique with a Zr-Si-N target. The RF power was set to 60W with a chamber pressure of 1.8×10^{-1}Pa. After lift-off process, device isolation is realized by UV/Ozone treatment for 15min using Zr-Si-N as the hard mask. Finally, the W gate was patterned on Zr-Si-N through standard photolithorgraphy and sputtering process. The schematic process of the MISFET is shown in figure 1. The MISFET with gate length of L_G=2μm, gate width of W_G=20μm and source-drain distance of L_{SD}=6μm was fabricated. The current-voltage and capacitance-voltage measurements were implemented at RT in a dark ambient environment by using Agilent B1505 A parameter analyzer.

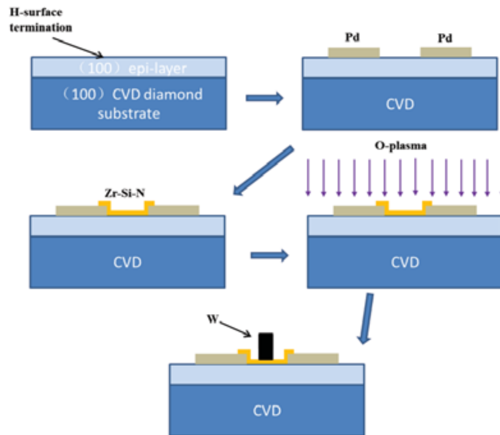

Figure 1. The schematic process of Zr-Si-N diamond MISFET

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DISCUSSION

Before the MISFET fabrication process, the quality of single crystal diamond is verified by Raman spectrum and X-ray diffraction (XRD) as shows in figure 2. According to the figure 2(a), the narrow symmetrical sharp peak can be seen at 1333.7cm^{-1}. The full width half maximum (FWHM) was measured to be 4.9cm^{-1}. From figure 2(b), the XRD rocking curve of the diamond epi-layer exhibits a sharp peak centered at 59.6981° with relatively low FWHM of 0.0093°. All data illustrates a high quality diamond layer.

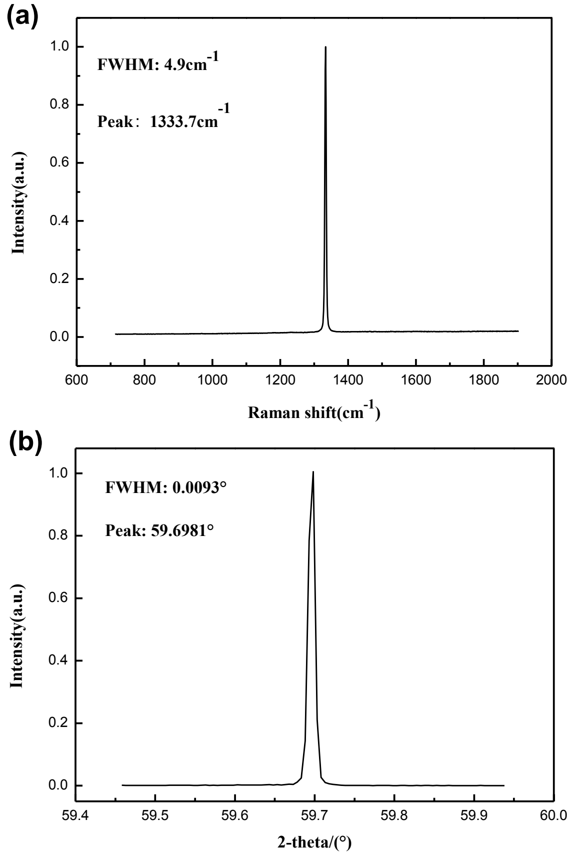

Figure 2. Characterization of single crystal diamond (a) Raman spectra; (b) X-ray diffraction rocking curve.

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The room temperature properties of the Zr-Si-N MISFET were investigated. Figure 3 shows the device DC drain current (I_{DS})–voltage (V_{DS}) characteristics with the gate voltage (V_{GS}) changed from 4V to -3V in step of -1V, where the drain current (I_{DS}) has been normalized with respect to W_G. As exhibited in figure 3, the $|I_{DS}|$ increases as the $|V_{GS}|$ increases, indicating that there is a p-type channel with hole-carriers under Zr-Si-N layer. It's the evidence that the 2DHG is reserved at the Zr-Si-N/diamond interface, which illustrates that the Zr-Si-N dielectric layer has the ability to preserve conduction channel on H-terminated diamond surface. Moreover, the surface channel FETs are depletion mode devices with normally-on characteristics.

The maximum value of drain current approaches -5.16 mA/mm, which is observed at the gate bias of -3V. The off-state I_{DS} is -3.84×10^{-6} mA/mm at the positive gate bias of 4V, manifesting the on/off ratio of 10^6 when gate bias is between -3V and 4V. It shows the ratio is high enough to practical applications. On resistance (R_{on}) of the device obtained from the linear part of the output characteristics is 589.5Ω·mm at the gate bias of -3V.

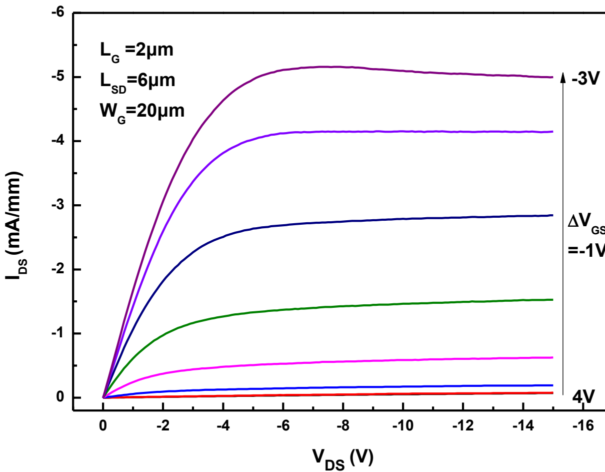

Figure 3. The room temperature DC drain current (I_{DS})-voltage(V_{DS}) characteristics of Zr-Si-N MISFET for various gate bias, with L_G=2μm, W_G=20μm and L_{SD}=6μm.

The values for the transfer and transconductance (G_m) characteristics, which were investigated at room temperature, are displayed in figure 4. A peak transconductance of 1.27 mS/mm is extracted from the curve measured at the source drain voltage of -0.44V. The V_{TH} of 3.0V is extrapolated from G_m-V_{GS} figure that once again verify the normally-on depletion mode.The subthreshold swing value was calculated to be 4180mV/dec.

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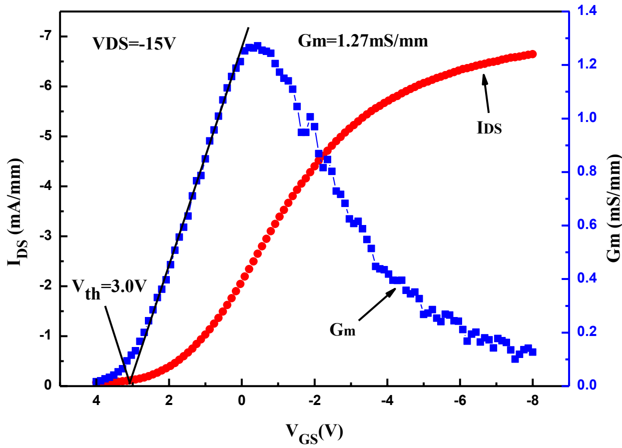

Figure 4. The room temperature transfer and transconductance (G_m) characteristics of Zr-Si-N MISFET for various gate bias, with L_G=2μm, W_G=20μm and L_{SD}=6μm.

The C-V characteristic curve for the Zr-Si-N diamond-based MISFET is shown in figure 5. The double sweeping mode was utilized to investigate the fixed and trapped charge at the Zr-Si-N/diamond interface. As one can see in the figure, the accumulation and depletion mode regions is readily observed. The sweep of capacitance began from negative bias. As the voltage is increased to -1.5V, the capacitance increases sharply. With further increment of the voltage to 0V, the capacitance begin to saturate. The maximum capacitance and the dielectric constant were calculated to be 0.275μF/cm^2 and 7.8, respectively.

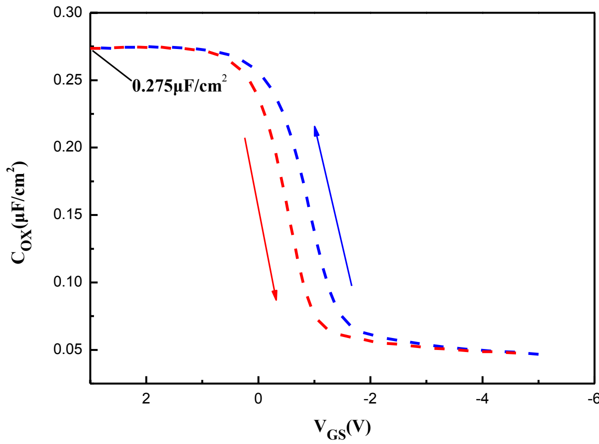

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Figure 5. The room temperature capacitance (C_{OX}) – voltage (V_{GS}) curve of Zr-Si-N MISFET. The gate bias sweep form negative to positive and followed by the opposite direction, respectively.

The relationship between effective mobility (μ_{eff}) and R_{ON} is expressed by the following equation[20].

$$R_{ON} = R_{CH} + R_{SD} = \frac{L_{eff}}{W_{eff} \times \mu_{eff} \times C_{OX} \times (V_{GS}\text{-}V_{TH})} + R_{SD} \qquad (1)$$

The R_{CH} is the channel resistance of the measured MISFET, R_{ON} is on state resistance, R_{SD} is the resistance including sheet resistance, spreading resistance and any other "wire" resistance. The effective channel length, effective channel width, capacitance of MISFET, gate bias and threshold voltage are represented by L_{eff}, W_{eff}, C_{OX}, V_{GS} and V_{TH}, respectively. The L_{eff} and W_{eff} are replaced by gate length (L_G) and gate width (W_G), approximately.

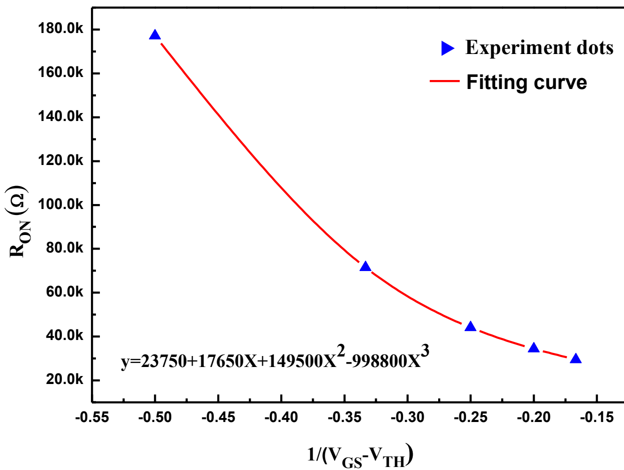

Figure 6. The R_{ON} versus $1/(V_{GS}\text{-}V_{TH})$ characteristics and their fitting curve. The dots is the experiment dots, and the curve is fitting curve.

By linear fitting of output curve ($V_{DS} \leq 0.3$), R_{ON} and $1/(V_{GS}\text{-}V_{TH})$ are considered as a function of the relationship and are shown in figure 6. By equation 1, it is concluded that R_{CH} is close to zero when V_{GS} tends to $-\infty$. Therefore, R_{SD} is calculated to be 23750Ω by three order polynomial fitting equation shown in figure 6. In equation 1, when the gate bias is of -3V, R_{CH} is calculated to be 29475Ω. Moreover, with the parameter of V_{TH} (3V), V_{GS} (-3V), C_{OX} (0.275μF/cm^2), μ_{eff} is obtained to be10.91 cm^2/(V.S), which is reasonable value for H-diamond epi-layer.

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CONCLUSIONS

In this study, passivation of diamond-based FET was realized by sputtering Zr-Si-N dielectric layer, and the performance of the device was fully investigated. The output and transfer characteristic both confirmed the presence of 2DHG at the interface. The fabricated Zr-Si-N diamond MISFET devices shows the threshold voltage of 3.0V, the maximum transconductance and drain current were 1.27mS/mm and -5.16 mA/mm, respectively. The on/off ratio of 10^6 is high enough for practical applications. The output properties of the devices illustrate a p-type channel at the Zr-Si-N/diamond interface, which indicates that Zr-Si-N dielectric layer has the ability to protect two-dimensional hole gas (2DHG). According to the C-V curve, the maximum capacitance and the dielectric constant were calculated to be 0.275μF/cm^2 and 7.8, respectively. The μ_{eff} is determined to be 10.91 cm^2/(V.S). Because of the excellent oxidation resistance, desirable properties, relatively low cost of Zr-Si-N film deposition, its application to the surface of diamond as dielectric layer of MISFET needs further study.

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