doi:10.1017/S1431927616003846
Microsc. Microanal. 22 (Suppl 3), 2016
© Microscopy Society of America 2016

How New Electron Detector Concepts Can Help to Increase Throughput and Sensitivity of Single- and Multi-Beam Scanning Electron Microscopes

A.Liebel[1], G.Lutz[2], U.Weber[1], M.Schmid[1] A.Niculae[1], H.Soltau[1]

[1]PNDetector GmbH, Otto-Hahn-Ring 6, D-81739 München, Germany
[2]PNSensor GmbH, Otto-Hahn-Ring 6, D-81739 München, Germany

Due to the growing utilization of electron microscopy in applications like soft matter analysis or in the semiconductor industry there is an increased requirement for instruments that enable fast scan rates at soft probing conditions. Additionally, instruments for industrial applications aim for higher throughput and new concepts such as multi column scanning electron microscopes have been emerging. All this demands for electron detectors which offer high sensitivity and detection speed as well as flexible designs. New readout concepts for solid state electron detectors could be the key technology for these modern instruments.

Silicon detector diodes for Backscattered Electron (BSE) imaging or Scanning Transmission Electron Microscopy (STEM) can be made very fast. The fundamental limitation of the detection speed is the signal collection time within the detector material. However, for many applications the available electron signals are weak and sensitive detector systems with high amplification are required. Hence, not only the detector bandwidth but the Gain-Bandwidth Product (GBWP) has to be large in order to obtain fast and sensitive detectors. Main limitations for this are parasitic capacitances within the readout chain. Stray capacitances due to cable connections can be reduced if a compact design for the detector assembly with optimum electrical interconnection is chosen (figure 1). The signal capacitance of the detector can be decreased by using an appropriate sensor chip material. Detection systems optimized in that way can achieve high detection speed. However, at some point technological limits are reached which can only be overcome by using an alternative detector concept.

We recently developed electron detector prototypes based on the principle of Silicon Drift Detectors (SDD) which have the potential to greatly increase the detector GBWP [1]. These current readout SDD structures make use of a very small collecting anode and therefore strongly reduced signal capacitance. Stray capacitances in the readout node are reduced to a minimum due to the implementation of the first amplification on chip-level. The concept makes use of a second sensor integrated Field Effect Transistor (FET) for the adjustment of the gain level. Signal rise times down to 40 nsec have been measured enabling artifact free imaging at scan speeds down to 25 nsec pixel dwell time (figure 2). More important, however, is the fact that the detector response remains fast even at very high amplification. Measured signal rise times at primary gain values of 10^9 V/A were still below 500 nsec which makes the detector more than 10 times faster than a conventional electron detector diode at similar primary gain.

Due to the integration of the first amplification stage onto the chip the subsequent electronics can be positioned with some distance from the detector outside the vacuum chamber. This way, the detector inside the microscope can be built very compact. It is also possible to combine several single cells to multi-cell sensors as exemplarily shown in figure 3. This could make this technology especially interesting for multi-beam instruments where several single electron signals have to be measured but the available space for the detector is restricted.

https://doi.org/10.1017/S1431927616003846 Published online by Cambridge University Press

We will present measurement results of detector structures with different sizes illustrating the benefits of this new technology with regard to throughput and sensitivity and give an outlook on how this technology could be used for compact multi-beam detection systems.

[1] A.Liebel et al., Microscopy & Microanalysis, vol. 20, S3 (2014), pp. 28-29

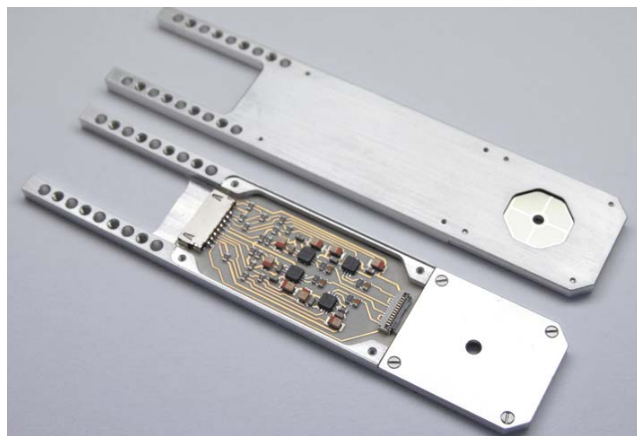

Figure 1. BSE Detector module with integrated preamplifier electronics. The compact design reduces stray capacitances of the electrical interconnection and enables signal rise times < 100 nsec.

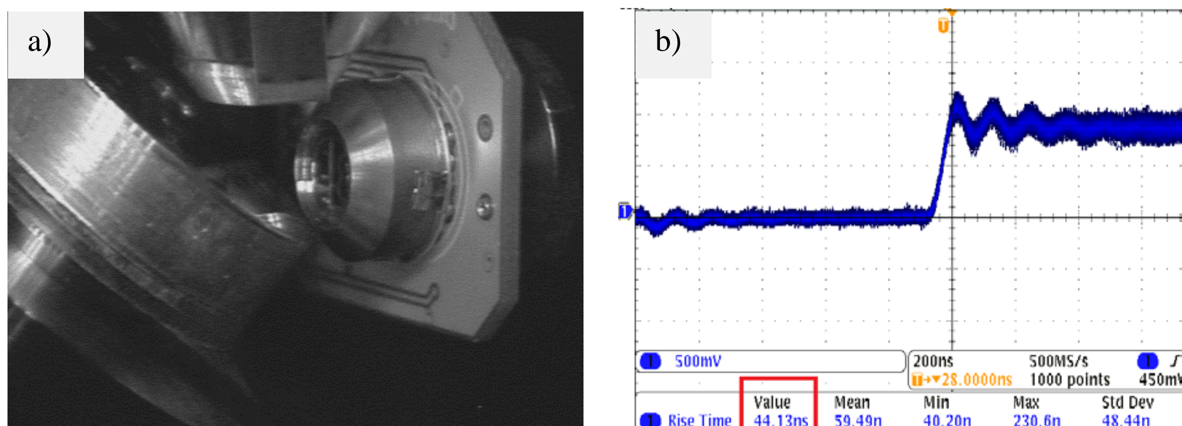

Figure 2. a) Current readout SDD test structure mounted in TO socket and installed inside an SEM in forescatter geometry. b) Knive edge measurements show signal rise times < 50 nsec.

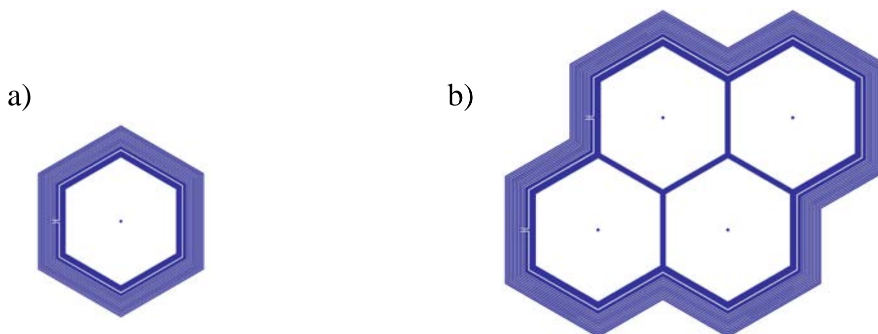

Figure 3. a) Geometry of a 5 mm² large current readout SDD test structure.
b) Exemplary combination of single cells into a multi-cell structure for multi-beam instruments.

https://doi.org/10.1017/S1431927616003846 Published online by Cambridge University Press