Design of a Multi-CCD Controller

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Abstract. We are developing a robust Multi-CCD control system for
wide-field surveys of various kinds. Our design concept and possible application modes are introduced.

1. Introduction

The YSTAR(Yonsei Survey Telescopes for Astronomical Research) project aims
to monitor the entire night sky for various transient events. As part of the effort,
we are developing a new CCD control system to increase the present YSTAR
survey capability in the future. The Multiple CCD Imaging System described
here is designed to use MPUs(micro processor units) and FPGAs(Field Programmerable gate Arrays). Our basic hardware components are modularized
so that each unit can control a CCD and the associated image processing; it is
easy to increase the number of modules as needed without modifying the main
control unit. Our control system is designed to be very flexible and capable of
serving observations of different nature. CCDs of wildly different characteristics
can be easily employed as the only needed change involves their clock pattern
files.

2. Design Goals

Our design goals are: (1) High speed control of very large image data using
DSP (TMS320C31) and MP (i80960), (2) Robust CCD control regardless of
the working wavelength and/or the characteristics of the CCDs, (3) Module
structure that allows for easy expansion as needed, (4) Real time basic data
process by hardware architecture, (5) Linux operation.

3. Discussions

Our system can be characterized by multipurpose, high-speed, parallel, and real-time control capabilities. It is also easy to expand into larger imaging system
as needed, either by mosaicing a number of CCDs into a single camera or by
linking several CCD cameras in parallel. Our module concept applies not only
to the control of CCD cameras, but also to the basic data processing. This
will enable very efficient data management of modern astronomical observations
which involve a very large volume of digital data.
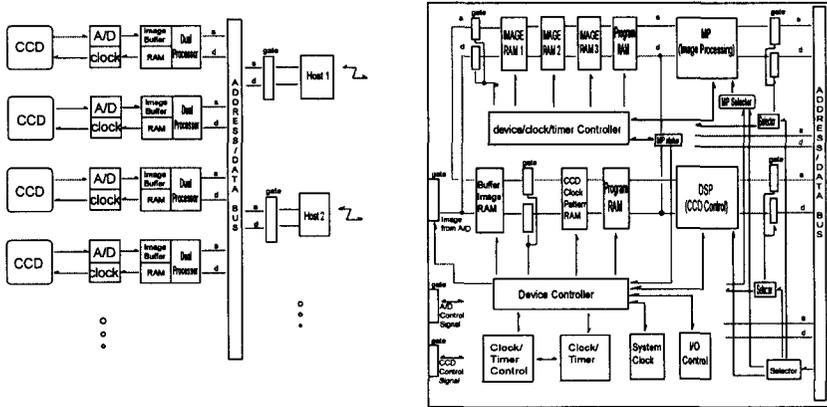
Figure 1.   Schematic diagram of our modulized CCD control system. Dual processors control the CCD and also perform basic image processing. The RAM contains clock pattern data, which are used to drive the CCD. The output signal gets converted to digital data and laced in the Image Buffer. Each module is interfaced with multiple hosts via the Address/Data Bus.
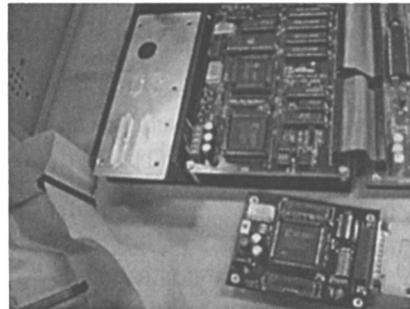
Figure 2.   (*Left*) CCD operation simulator. It generates imaginary A/D signals and forwards them to an image buffer. It also takes the clock pattern from computer and forwards it to the CCD clock driver. (*Right*) The Multi-CCD controller during development. The top unit is responsible for DSP and CCD control. We are developing algorithms for device control signals between different parts based on FPGA. The bottom unit is for MP image processing development.