Silicon Carbide Replaces Beryllium for Airborne and Space-Based Optics

In space-based remote sensing applications, it is desirable to have lightweight instruments that can be launched into orbit with small, low-cost rockets, resulting in a major cost reduction for the mission. Beryllium, which is highly toxic, has been used to fabricate optical mirrors used in satellites because its specific stiffness (Young's modulus divided by density) enables the production of extremely lightweight, stiff optical systems. SSG Precision Optronics Inc. is fabricating lightweight mirrors for space-based optical systems and remote sensing applications from silicon carbide (SiC), a ceramic material that is both nontoxic and more thermally stable than beryllium. SiC is also readily available, whereas Be is expensive and limited in availability.

SiC offers a mix of properties that make it an attractive candidate for these applications. It provides a specific stiffness that is 70–90% that of beryllium (depending on the material formulation and manufacturing approach) while maintaining a thermal stability (i.e., thermal conductivity divided by the coefficient of thermal expansion) that is better than ultralow-expansion (ULE™) glass. SiC can be used to produce lightweight, stiff, thermally stable optical systems using manufacturing processes that reduce the costs associated with more traditional materials such as ULE glass and beryllium and avoid the health risks that are specifically associated with beryllium.

For SiC materials to become more acceptable for these applications, several technical issues need to be resolved. Mirror substrates must be produced that are extremely lightweight; reflective optical surfaces must be polished to tight surface-figure-error (the difference between the desired and actual optical profile) and microroughness requirements; structural elements must be robust, durable, and tough in order to withstand the stress of launches; and the attachment approaches used need to be compatible with brittle ceramic materials.

SSG has been developing technologies for these purposes. A near-net-shape slip-casting approach is used to obtain extremely lightweight rib-supported mirror structures. In glass, these types of lightweight structures can be produced with a combination of machining, chemical etching, and high-temperature fusing. None of these approaches is suitable for SiC since the material's brittleness and high hardness (Knoop) make machining slow and costly, while its inertness makes it almost impossible to chemically mill. SSG's near-net-shape manufacturing process begins with a slurry of SiC particles and water. This viscous slurry is slip-cast into a mold, which produces a 70–85% "lightweighted" mirror substrate with almost no machining. The SiC mirror is fabricated with ribs on the back that support a face sheet, as compared with an unsupported, or "slab-type," mirror. The resulting mirror is lighter because sizable portions of the SiC material have been removed.

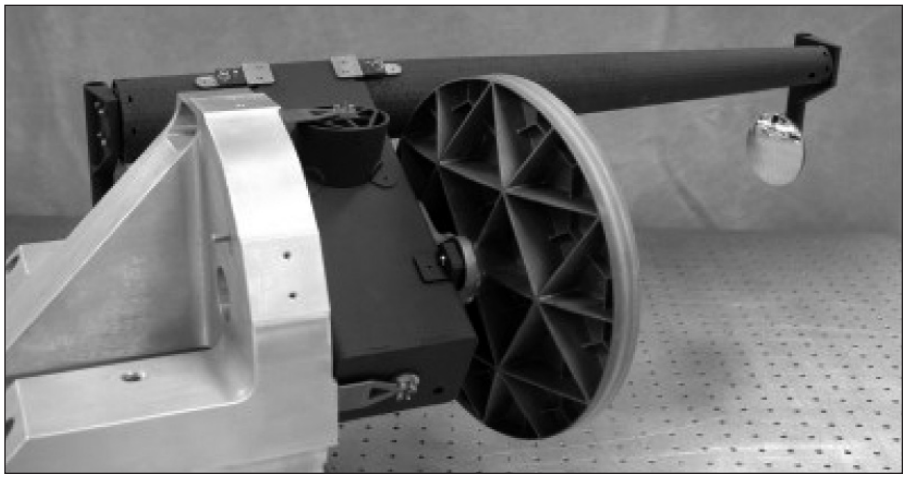

Figure 1. The SiC telescope developed by SSG Precision Optronics for the geosynchronous imaging Fourier transform spectrometer (GIFTS) space flight mission.

The polishing of high-quality, aspheric optical surfaces (a surface profile that is neither flat nor spherical) into the SiC material has been demonstrated by Tinsley Laboratories, a subsidiary of SSG. The company's proprietary computer-controlled optical surfacing (CCOS) processes have been refined to grind and polish SiC. Aspheric SiC mirrors with surface figure errors as small as 7 nm rms and optical finishes of 0.5 nm rms have been demonstrated.

The requirement for a durable structural material has been met by developing a composite that is reinforced with SiC fibers. A continuous fiber composite has been demonstrated and qualified for space flight, and a chopped fiber material is currently being developed. Both materials can be used to produce a durable optical metering structure whose coefficient of thermal expansion is matched to the slip-cast SiC. The combination of these two technologies provides a telescope with dimensions that do not vary with the temperature and that therefore is suited for application in dynamic thermal environments. The integration of SiC components into an optical system has been resolved by epoxy bonding, metallic brazing, and ceramic fusing.

Figure 1 shows a photo of the SiC telescope for the geosynchronous imaging Fourier transform spectrometer (GIFTS) that SSG has recently developed for Utah State University's Space Dynamics Laboratory in support of NASA's New Millennium Program. GIFTS has been developed as a next-generation spectrometer demonstration for remote sensing weather satellites. The system demonstrates the readiness of all of the technology elements: slip-cast mirror substrates, CCOS polished optical surfaces, fiber-reinforced SiC structures, and specialized joining techniques.

Opportunities

SSG Precision Optronics is interested in the development of new technologies that can provide additional benefits to its SiC materials technologies.

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Lab-On-a-Chip Analytical Systems Use Microfluidic Devices with Porous Polymer Inserts

The rapid development of microfabricated analytical devices is driven by the need for significant improvements in speed, sample throughput, cost, and handling of analyses. A variety of applications such as sensors, chemical synthesis, and biological analysis have been demonstrated using microfluidic chips. Work is under way on fabricating complex micro-total-analysis systems (μTAS) (called "lab-on-a-chip") by combining a variety of functional building blocks within the chip. However, most current approaches to μTAS rely largely on the use of open channels. Open channels have only small surface area available for desired interactions. Researchers at E.O. Lawrence Berkeley National Laboratory (LBNL) have developed preparation processes triggered by ultraviolet light that create porous polymer monoliths (i.e., a single, continuous piece of a polymer prepared using a simple molding process) with both controlled porous properties and surface chemistry located within the channel of the microfluidic device. The monolith affords a much larger surface area than open channels. In many applications, a specific type of surface chemistry is required to achieve the desired interaction. In addition, the monolithic material must also be porous to allow the flow of liquids. The methods of the scientists at LBNL significantly increase the available surface area and enable the fabrication of efficient building blocks.

Rigid porous polymer monoliths are used in a broad range of applications that exploit the ability of their pores to allow gases and liquids to pass through at low applied pressures. In contrast to typical processes that depend on diffusion (for example, chromatography in packed beds), processes using monoliths are considerably accelerated if convective mass transfer is facilitated by flow through the pores.

Monolithic materials with well-controlled porous properties are prepared by *in situ* polymerization within the confines of a cavity that acts as a mold. For example, the channel of a microfluidic chip can be used as the mold. To prepare the porous polymer in the microfluidic chip, the channel is first filled with a liquid precursor, a mixture of monomers, initiator, and inert solvents that help produce the desired pores. Next, a mask that is opaque to UV light is placed over the chip. This mask has a window that exposes the desired portion of the channel. The polymerization mixture is then irradiated with UV light through the mask to trigger the polymerization process, which produces a solid, porous, monolithic material that completely fills the cross section of the channel.

Several building blocks for μTAS advantageously use these monolithic materials. Chromatographic separation columns, static mixers, pre-concentrators, electro-osmotic pumps, and solid-phase extractors in glass chips have already been demonstrated. For example, a microchip containing a short plug of a hydrophobic monolith adsorbs compounds from very dilute solutions that are then released in a much smaller volume with their concentration increased well over 1000 times.

The use of thermoplastic polymer materials, together with relatively low-cost dry techniques such as injection molding or hot embossing, eliminates the costly multistep wet fabrication for these microfluidic devices. Because of the generally poor material compatibility of most polymeric materials, the monoliths tend to debond from the walls of plastic devices, forming voids at the monolith–channel interface, which then makes the devices ineffective.

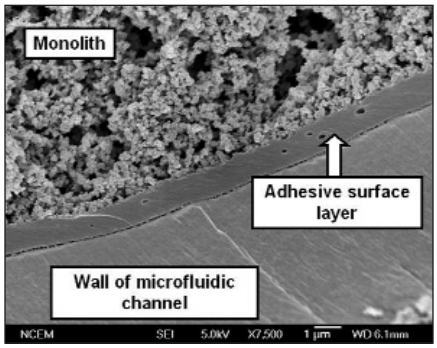

Figure 1. Scanning electron micrograph showing the cross section of a porous polymer monolith inside a delaminated microchip fabricated in a cyclic olefin copolymer (COC).

The LBNL researchers solved this problem by developing an approach combining UV-initiated grafting with a divinyl monomer that provides the channel surface and a thin grafted layer of polymer with a multiplicity of pendent double bonds, which are then used in the next step for covalent attachment of the monolith to the wall. Figure 1 shows an image (top view) of porous polymer monoliths inside a channel fabricated in a cyclic olefin copolymer (COC) microchip, which confirms that the monolith is firmly attached to the COC wall.

In order to significantly augment the number of functionalities located at the pore surface within the monolith, the researchers have also implemented the controlled UV-initiated grafting of chains of functional polymers within the pores of porous polymer monoliths. This approach enables the formation of layers of contiguous segments with different chemical functions and even the production of monoliths with a gradient of functional groups. This provides versatile access to permeable materials with both tailored surface chemistries and the incorporation of controlled functionalities. The grafted materials possess a high loading of the functional group, which makes them of interest for a variety of microfluidic applications including catalysis, capture, molecular recognition, immobilization, and separation.

Opportunities

This technology, which can be used for the fabrication of complex microfluidic devices in which the presence of a material with a large surface area and/or specific functionality or combination of functionalities is desired, is available for collaborative research and licensing.

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Double-Gated Transistor Aims to Reduce Chip Processing Costs

Silicon-on-insulator (SOI) chip processing has decreased the amount of power needed to run electronic devices such as wireless phones; however, this improved performance is relatively costly, which has limited its widespread adoption. A device called Flexfet™, developed by American Semiconductor Inc. (ASI), can operate on less than 1 V, whereas similar devices operate between 2.5–3.3 V. Flexfet was demonstrated at the University of California—Berkeley Microlab, under the direction of ASI's engineering group. Production transfer is scheduled for late 2004. This device is expected to improve performance and reduce the cost of chip processing relative to conventional technology.

Flexfet's transistor architecture is the key. Double-gated transistors are incorporated in the devices. These independent, fully self-aligned top and bottom gates within a four-terminal, sublithographic structure enable dynamic threshold voltage control of individual transistors and circuits. This configuration allows dynamic optimization of speed and power for commercial ultralow-power RF, analog and digital circuits. Flexfet technology is of particular interest for aerospace applications due to inherent radiation tolerance for total ionizing dose (TID) in excess of 1 Mrad. It is suitable for extreme radiation and thermal applications as well as advanced system-on-chip, readout integrated circuit, and imager solutions for space and high-altitude components. Mask and processing costs are lower than for competing complementary metal oxide semiconductor (CMOS) technologies. Fewer and less costly masks are required to make Flexfet CMOS and the new process has fewer fabrication steps than standard CMOS technology.

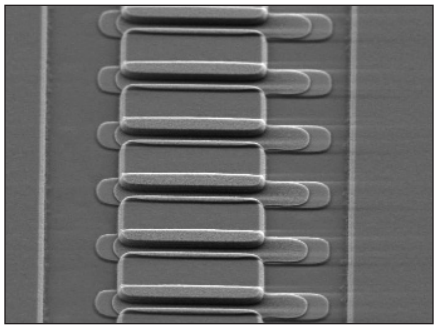

Figure 1. Scanning electron micrograph showing an interdigitated Flexfet device with self-aligned TiN top and silicon bottom gates in trenches between source/drain mesas; image made prior to local interconnect and metallization.

Flexfet is a planar transistor with a self-aligned silicon bottom gate, damascene metal (metal formed in trenches using chemical–mechanical processing) top gate, and a dual-damascene metal local interconnect. The technology allows circuit designers to mix and match six device modes in the same circuit on the same chip, to dynamically adjust threshold voltage, and to drive current/speed and leakage/power on a transistor-by-transistor basis during chip operation, thereby enabling designers to create new products.

The dynamic threshold (DT) mode is useful for ultralow-voltage 0.5–0.8 V circuits (particularly analog/RF). The lateral bipolar junction transistor mode is a connection for bandgap reference, low noise, and other analog applications. The grounded body mode is the conventional SOI device. The reverse-dc-biased bottom gate reverse bias mode is a high-V_t (threshold voltage, the voltage at which a transistor turns on) low leakage device for low-power dissipation or dynamic storage. The forward-dc-biased bottom gate mode is a low or zero-V_t, very high performance device, and the independently-double-gated mode with separate ac signals can be used for unique new functions, such as single-devices or gates and single-device mixers.

An interdigitated Flexfet is shown in Figure 1. This structure incorporates low-series-resistance thick source/drains (S/Ds) with a relatively thick 100–200 nm SOI layer forming a gate trench to the desired channel thickness. This avoids the cost and complexity of starting with an ultrathin SOI film and growing selective epitaxially deposited raised S/Ds following gate formation. In the raised S/D process, the implanted source/drain extension junctions are subjected to the thermal budget for epitaxial growth and cannot be kept as shallow as required. American Semiconductor's thick S/D mesas are implanted and annealed before the formation of the ultrashallow junction. The gate trench is etched through these deep S/Ds, recessing the channel into the underlying undoped region, as shown in Figure 2. Flexfet technology allows high-κ gate dielectrics and work-function-engineered metal gates to be deposited and planarized in the gate trench, thereby avoiding high temperature exposure for thermally-sensitive gate materials (e.g.,

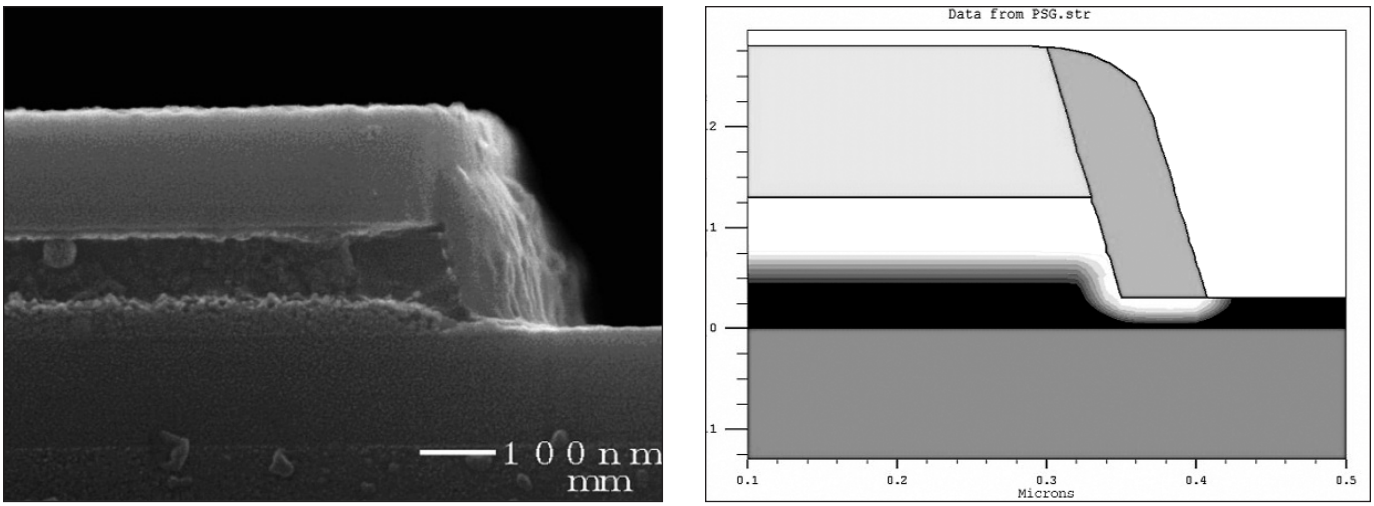

Figure 2. Ultrashallow source/drain extensions (a) micrograph and (b) schematic.

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HfO_2, TiN, lead zirconium titanate, and barium strontium titanate, aluminum, and copper). Etch plasma damage does not occur to the gate dielectric/channel edge since the gate is not plasma-etched but, instead, planarized into a gate groove/trench. This structure is expected to facilitate new stacked gate architectures for nonvolatile memory applications. A unique dual-damascene local interconnect is embedded into the shallow isolation trenches that run in between source and drain SOI mesas. It is used to connect to bottom gates, top gates, and source/drains. The local interconnect routes signals across relatively long distances by running in the same shallow isolation trench normally used for isolation between devices.

The device is fabricated using a sublithographic technology. Minimal physical features are created that can be beyond the capability of photolithography (e.g., a 65 nm feature printed in Flexfet could generate a 30 nm physical feature). Sub-50 nm channel lengths can be fabricated with 100 nm node process tooling, and 150 nm channel lengths can be fabricated with 0.35 µm process equipment. Fabrication capability is enhanced by providing greater than double the improvement in minimum channel length without any significant equipment upgrades or capital investment.

Opportunities

ASI is seeking collaborations with Original Equipment Manufacturers, Integrated Device Manufacturers, chip designers, and CMOS fabricators interested in using their foundry capabilities or in licensing the Flexfet technology.

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