Microsc. Microanal. 8 (Suppl. 2), 2002
DOI 10.1017.S1431927602107926

© Microscopy Society of America 2002

A Novel Method for Direct TEM Study of Microstructure of Polysilicon Films Crystallized with and without Underlying Oxide

Xiang-Zheng Bo[1], Nan Yao[2], James C. Sturm[1]
[1] Center for Photonic & Opti-Electronic Materials, Princeton University, Princeton, NJ 08544
[2] Princeton Materials Institute, Princeton University, Princeton, NJ 08544

The demand for high quality semiconductor sample preparation for high-resolution TEM analysis is rising sharply as the critical dimensions of integrated circuits continue to shrink down further into the sub-micron regime. A well-prepared sample with accurate defect localization and endpoint control of final sample thinning is necessary for getting meaningful results. Conventional techniques including mechanical dimpling, ion milling, focused ion beam milling and wedge mechanical polishing have drawbacks for semiconductor thin film samples due to their lack of sub-micron precision polishing and/or ion beam damage control. In this paper we present a novel method that combines TEM sample preparation with thin film fabrication. Plan-view TEM samples of polysilicon films are prepared simply by a dissolving the underlying oxide to free the films without any grinding or milling. The method is used to study the effect of the underlying oxide on the crystallization process.

Since polycrystalline silicon films transited from amorphous silicon via solid phase crystallization (SPC) are active layers of thin film transistors (TFTs) in AMLCD, investigation of polysilicon microstructure is important for the improvement of TFT performance. A cantilever structure was designed to reduce the defects inside grains [1], so that films could be crystallized to polysilicon free from the influence of the underlying Si/SiO_2 interfaces. Figure 1 shows the fabrication process of such a silicon cantilever. First, a 60nm-thick PECVD *a*-Si film (Fig. 1(a)) was patterned into islands by optical lithography and dry etching (Fig. 1(b)). Diluted HF etching created cantilever suspension (Fig. 1(c)) by removing SiO_2 under the cantilever. SEM micrograph (Fig. 2) confirms silicon cantilevers lying above the substrate. After furnace anneal at 600 ?C for 24 hr, *a*-Si film is fully crystallized into polysilicon. TEM sample preparation process is shown in Fig. 3. Cantilever sample was first dipped into a concentrated HF solution, which has high etching selectivity of silicon oxide over silicon. Thus underlying oxide was fully etched away; the silicon film was peeled off in the solution and subsequently picked up using a copper grid (Fig. 3(b)). Microstructure of a polysilicon grain in the control region (where the underlying oxide was not removed prior to crystallization) was shown in Fig. 4(a). Defects, such as microtwins and dislocations, are very evident. The average defect-free area is reduced to 25 nm in diameter, which is in consistent with the observations in Ref. 2. However, in the cantilever region, bright-field plan-view TEM observation (Fig. 4(b)) shows less intragranular defects within a <110> oriented grain indexed from the diffraction pattern (inset of Fig. 4(b)). The defect-free area increases to ~100 nm in diameter on average. High-resolution TEM observation (Fig. 4(c)) on the marked region in Fig. 4(b) shows the atomic arrangement around the coherent microtwins. On both sides of the microtwins, periodic {111} planes without any defects are clearly seen. This reduction of defect density is thought due to the stress from SPC relieved by removing the underlying oxide [1].

References
[1] X.-Z. Bo et al, J. Appl. Phys. accepted for publication (March, 2002).
[2] L. Haji et al, J. Appl. Phys. 75 (1994) 3944.

https://doi.org/10.1017/S1431927602107926 Published online by Cambridge University Press

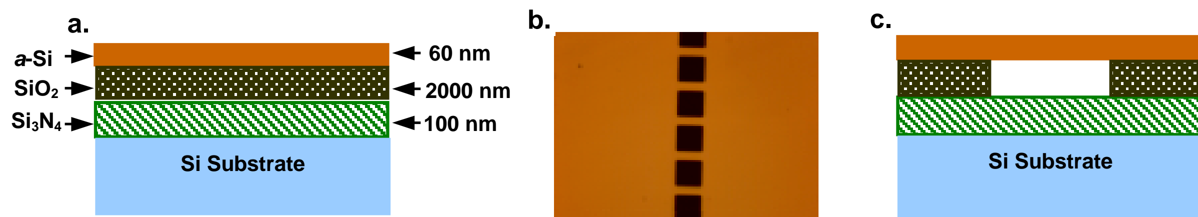

Fig. 1. Fabrication process: (a) layer structure; (b) top view of cantilever after optical lithography and dry etching; (c) underlying oxide etch to form the cantilever.

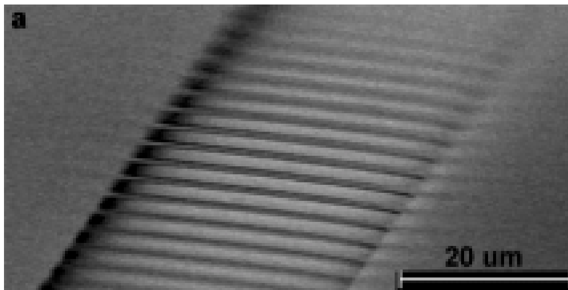

Fig. 2. SEM observation to confirm the suspension of the cantilever on the substrate.

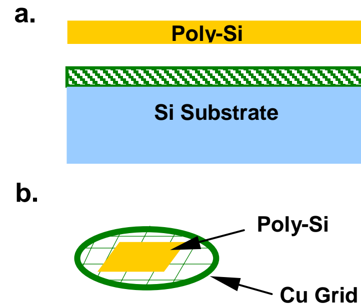

Fig. 3. TEM sample preparation: (a) Film peeling off by selective wet etching, and (b) picked up by copper grids.

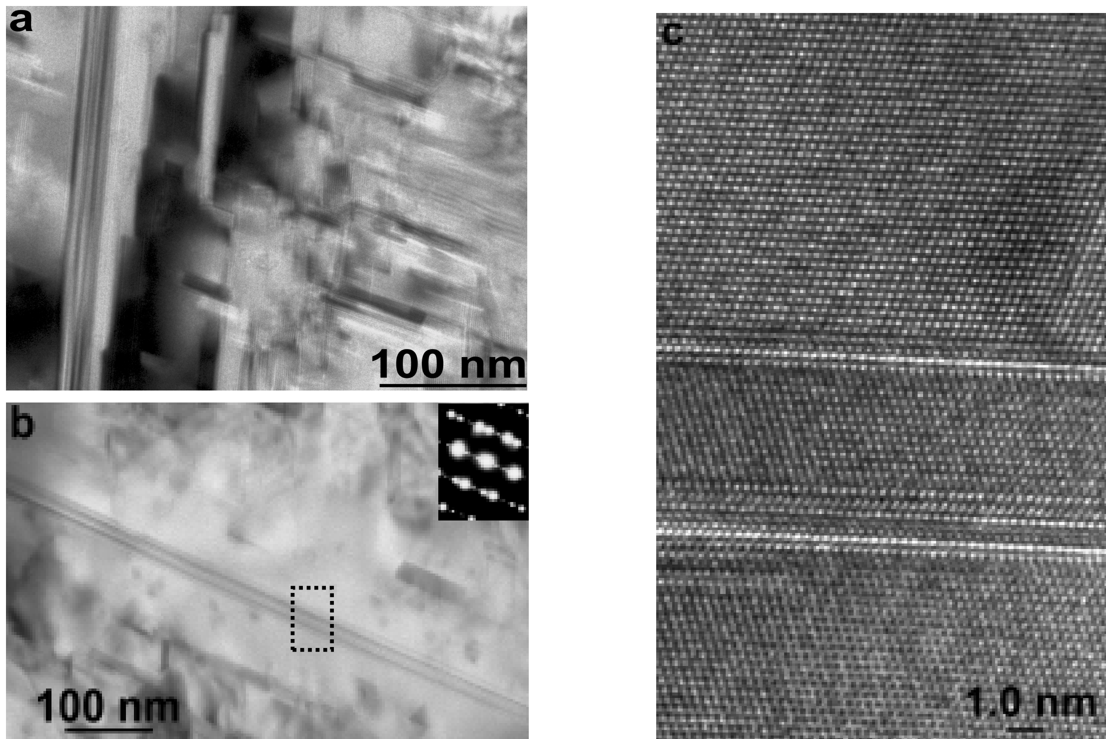

Fig. 4. Microstructure of polysilicon grains oriented with <110> to show the defect density in (a) control sample and (b) cantilever sample. High-resolution TEM observation of (c) from the marked area in (b) to show the perfect atomic arrangement on both sides of the microtwin.

https://doi.org/10.1017/S1431927602107926 Published online by Cambridge University Press