doi:10.1017/S1431927616001835
Microsc. Microanal. 22 (Suppl 3), 2016
© Microscopy Society of America 2016

# Curtaining-Free Top-Down TEM Lamella Preparation from a Cutting Edge Integrated Circuit

Andrey Denisyuk[1], Tomáš Hrnčíř[2], Jozef Vincenc Oboňa[2], Martin Petrenec[2] and Jan Michalička[1]

[1.] TESCAN ORSAY HOLDING, Libušina třída 21, Brno, Czech Republic
[2.] TESCAN Brno, Libušina třída 1, Brno, Czech Republic

Semiconductor industry continues to shrink sizes of the electronic devices. Currently commercial state-of-the-art technology node for integrated circuits is 14 nm, while 10 and 7 nm technology nodes are in the development stage [1]. Those integrated circuits are based on multigate transistors, where source-drain channel ("fin") is surrounded by a 3D gate. Failure analysis process of such integrated circuits typically involves inspection of TEM lamellae prepared by FIB-SEM machines from a single transistor layer. One difficulty in preparation of such lamellae is different ion milling rates of materials of the integrated circuits. In case of conventional top-down FIB polishing this causes unwanted curtaining artefacts resulted mainly from the metal contacts above the transistor layer. One way to eliminate curtaining is so called backside (or inverted) polishing technique which involves lamella extraction, flipping and polishing by FIB through the silicon layer [2]. However, this technique is too much time consuming for a daily semiconductor industry process.

In this talk we present a new technique of curtaining-free lamella preparation. This technique allows for normal top-down FIB polishing through upper metal contacts while curtaining artefacts are eliminated due changing the incident angle of ion milling by rocking of the sample on a special stage.

In order to demonstrate this technique, we took the latest commercially available processor based on 14 nm technology node [3] (Intel Pentium G4400). The processor wafer was decapsulated and mechanically polished to remove the top metal contacts. Further delayering was performed by means of a specially developed technique of water-assisted Xe Plasma FIB etching. The later technique allows uniform damage-free delayering down to the first metal layer which is just above the transistor layer (Fig. 1a). The delayered sample was transferred to a FIB-SEM machine which was equipped with a Ga FIB column, an SEM column with immersion optics and a Rocking stage [4].

Initial steps of a lamella preparation involved a standard routine of Pt protection layer deposition, FIB trench milling, undercut and lamella transfer by a nanomanipulator to a TEM half-grid for the final thinning. Lamella thinning was performed by Ga FIB at 30 kV till reaching the lamella thickness of 150 nm. The last step of thinning down to the thickness of less than 20 nm was performed by 5 and 2 kV FIB polishing (see perpendicular "fin-cut" for illustration on Fig. 1b). The final lamella was prepared just in the middle of a single fin (so called "gate-cut"). Importantly that during the last steps of FIB thinning the lamella was milled from two directions on the Rocking stage (Fig. 2a). So due to continuous change of Ga beam incident angle (±15º) curtaining artefacts were eliminated.

Finally, the prepared lamella was transferred to a TEM microscope for observation. The observation demonstrated that even though the lamella was polished by Ga FIB by top-down technique through upper metal contacts it does not show evidence of any significant curtaining artefacts (Fig. 2b). The demonstrated result proved the potential of the technique of top-down lamella thinning on a Rocking stage.

https://doi.org/10.1017/S1431927616001835 Published online by Cambridge University Press

References:
[1] http://www.itrs2.net/
[2] O Ugurlu, M Strauss, G Dutrow, J Blackwood, B Routh, C Senowitz, P Plachinda, and R Alvis, Proc. of SPIE **8681** (2013), p. 868107.
[3] http://www.intel.com/content/www/us/en/silicon-innovations/intel-14nm-technology.html
[4] T Hrnčíř, J Dluhoš, L Hladík, E Moyal, J Teshima, and J Kopeček, 40th ISTFA Conf. Proc. (2014), p. 136.

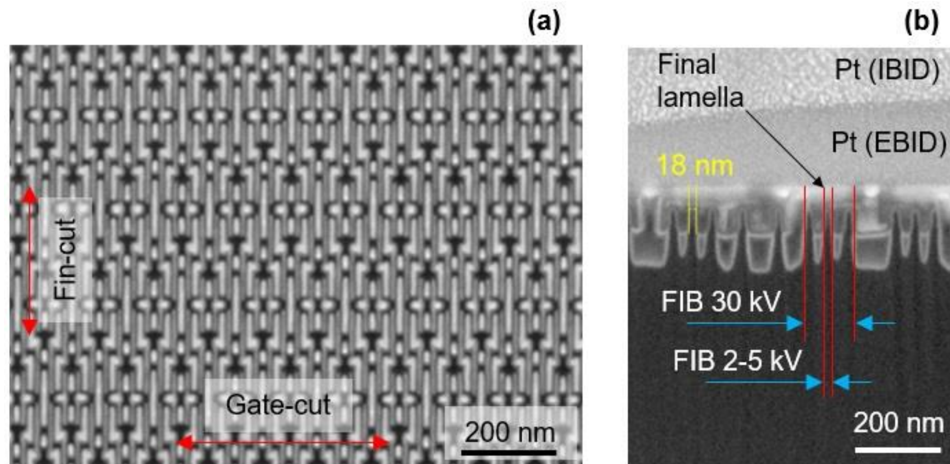


**Figure 1.** Top view image of the first metal layer after delayering by water-assisted Xe Plasma FIB etching (a). "Fin-cut" of the chip illustrating the place and procedure of further lamella thinning (b).

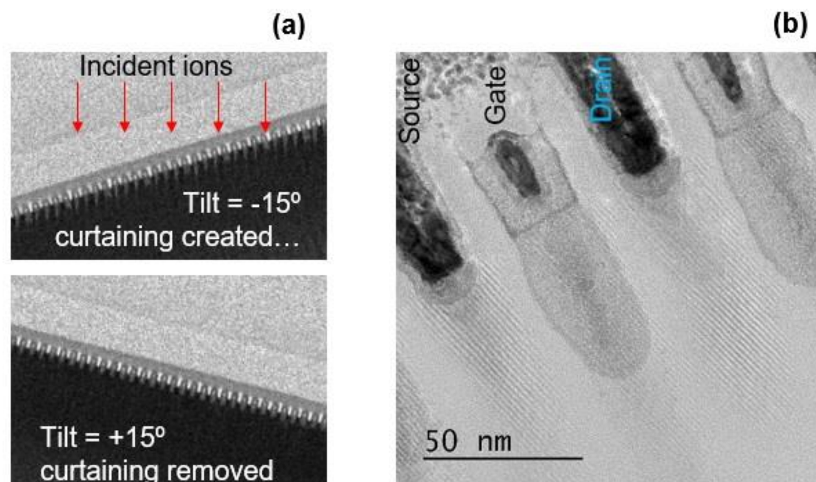


**Figure 2.** Thinning the lamella on a Rocking stage: altering the ion incident angle by ±15º eliminates curtaining (a). TEM image of the lamella prepared in the middle of a single fin ("gate-cut") shows no significant evidence of curtaining artefacts (b).

https://doi.org/10.1017/S1431927616001835 Published online by Cambridge University Press