CCD CONTROLLERS

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ABSTRACT: The requirements of current and next generation CCD controllers in the areas of CCD device and system architectures, readout noise, number and speed of readouts are reviewed together with such operational requirements as system flexibility, power consumption, cost and weight. The basic components of a CCD controller are described, including the timing sequencer, clock drivers, video processor and computer interface. The capabilities and implementation of the CCD controller developed at San Diego State are reviewed. An upgraded controller is described to overcome limitations in the area of readout speed and efficient support of multiple readout capability.

1. INTRODUCTION

Improvements in the quality of CCDs developed within the last several years have brought about a corresponding change in the requirements of the controllers used to operate them in ground based optical observatories. The proliferation of different CCD device geometries and readout requirements brought about by the manufacture of CCDs by silicon foundries has led to a much better match of the CCD to its associated optical instrumentation, and has inspired a corresponding improvement in the versatility of their controllers. A parallel decline in the cost of CCD devices has enabled the construction of instruments with more than one CCD, while the increased number of pixels per CCD and the implementation of multiple readout circuits on a single CCD have motivated the development of multiple readout controllers.

Several groups (Reiss 1995, Bonanno 1995, Glass et al. 1995, Leach 1994) have met this challenge by designing controllers containing micro-processors to control the CCD waveforms, clocking voltages and image data flow. This allows considerable operational flexibility since the microprocessor program can be easily changed from the host computer. Different programs can be stored in the host computer for operating different geometry CCDs, for operating the same CCD with different sets of voltages and timing waveforms or readout modes, or to reflect various stages in the developer's understanding of how to optimally operate a given sensor. These controllers are referred to as programmable controllers, as opposed to fixed format or static controllers.

Section 2 below discusses how programmable controllers are implemented, reviewing their general characteristics and architecture as currently implemented in ground based astronomical observatories. Section 3 presents some specific operational parameters of the current programmable controller developed by the author and his colleagues at San Diego State University, and discusses some issues that are motivating a planned upgrade whose design is underway.

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2. CURRENT CONTROLLERS

Table 1 lists some of the characteristics of current programmable controllers, and reflects in a general way the four controllers discussed in references mentioned in the second paragraph. Programmability of CCD waveforms and voltages can lead to efficient and reliable system development since electrical components do not have to be removed from the system. Versatile readout reflects not only the diversity of CCDs to be operated but the optimal readout of a given geometry to reflect the astronomical requirements of a particular observation - binning or summing charge from adjacent pixels in either the horizontal, vertical (or both) directions before readout will degrade image resolution but improves the signal-to-noise ratio and can be useful in low signal observations. Reading out only the portion of the CCD that is actually usefully illuminated can reduce the readout time and the image data quantity, while similar gains can be achieved with region-of-interest readouts that select several non-contiguous regions within the CCD field for readout. Region-of-interest readout is particularly useful for observations of small numbers of stars, especially for time variability studies. Multiple readout of several CCDs allows a large increase in image sensor area to accommodate large focal planes, while multiple readouts on a single CCD is useful for reducing the total readout time for the array, an issue increasingly important as CCDs contain more and more pixels. An integrated host computer for loading controller programs, processing user commands, and for storing image can lead to efficient instrument operation and is useful for properly configuring instrument configurations.

TABLE 1

Current Programmable Controller Characteristics

In-situ programmability - CCD waveforms, voltages and readout modes. Versatile readout - binning, sub-image, region-of-interest, multiple readouts. Integrated host computer - for loading controller programs, processing commands, displaying images and image storage.	
Max. readout rate	10 μsec/pixel
Dynamic range	determined by A/D, 16-bits normal 20-bits with special effort
Readout noise	dominated by CCD
Weight	few Kg.
Cost	US $10 - 20k
Power dissipation	< 30 watts
Availability	Some commercially, some not

Quantitative characteristics are harder to discuss since they vary quite a bit amongst the programmable controllers. A maximum readout rate of ten microseconds per pixel to 16-bit accuracy reflects the availability of an inexpensive and compact monolithic CMOS A/D converter manufactured by Crystal Semiconductors, and is sufficient for slow scan readout of currently available CCDs for obtaining readout noise figures down to two electrons rms.

Readout noise is dominated by the CCD even for readout noise values around two electrons rms since they are achieved either with CCDs with high gain on-chip source followers or by long signal integration times. Sixteen bits dynamic range is fixed by the available A/D converters, not by the CCDs, since the dynamic range of some CCDs exceeds 10^5, especially if binning is implemented. Controller dynamic range can be extended to 20 bits by dynamically switching to a low gain analog processing stage ahead of the A/D converter for pixels with high signal levels where the photon shot noise exceeds the digitization error, and then multiplying its A/D counts by the ratio of the gains of the high and low gain stages (Reiss 1995).

Current controllers weigh a few kilograms, including power supply and enclosure, cost somewhere around US $10 - 20 k if a proper accounting of labor charges is made, and dissipate something less than 30 watts, sometimes even less than 10 watts. These properties are entirely suitable for ground-based systems, especially since the cost of the controllers is a small fraction of the cost of CCD sensors typically implemented. Some of these programmable controllers currently in use are available commercially, and some are not.

Fig. 1 shows a block diagram of a typical CCD controller configured for a single readout. A sequencer generates digital waveforms for controlling the clock driver, which translates them into low impedance analog voltages connected to the CCD. A video processor amplifies, filters and digitizes the output of the CCD, which then goes over the communications link to an optional intermediate image memory. This is required in some systems to ensure that images are not damaged by slow host computer response times in multitasking environments. A host computer interfaced to the image memory serves as the user interface, image display, storage medium, and, often, the detector development systems as well. A housekeeping function is included in many system to perform tasks not directly related to CCD control such as shutter timing and control, CCD temperature control, power control and overall system monitoring.

Multiple readout capability is illustrated in Fig. 2 wherein the analog functions of the clock driver and video processor are shown replicated four times for a four readout system. The video processor is replicated because the readout speed for slow scan, low noise astronomical systems is generally limited by the sampling time of the video signal, since the largest noise contribution is usually from white (Johnson) noise of the on-CCD source follower FET. Installing one video processor to each readout allows the video sampling for all readouts to occur simultaneously, so the array readout time is reduced by the number of readouts while still allowing enough time for adequate signal integration time to get low readout noise. The clock driver circuits need to be replicated only as many times as are required to drive the CCD clock driver and DC bias pins in the readout configuration desired. When driving a single CCD with multiple readouts some savings can be realized by driving the parallel and serial transfer registers for each quadrant in parallel, though the readout circuits associated with each on-chip amplifier should be driven separately to minimize crosstalk problems between the readouts. The timing, housekeeping and communication portions of the controller are generally not replicated for modest numbers of readouts since they are constructed mostly from digital circuit components whose bandwidths exceed the video processing bandwidth by enough factors that they can multiplex between the video processors and clock drivers. This can recuce the system cost though it also sets the upper limit to the number of readouts that can be incorporated in a system.

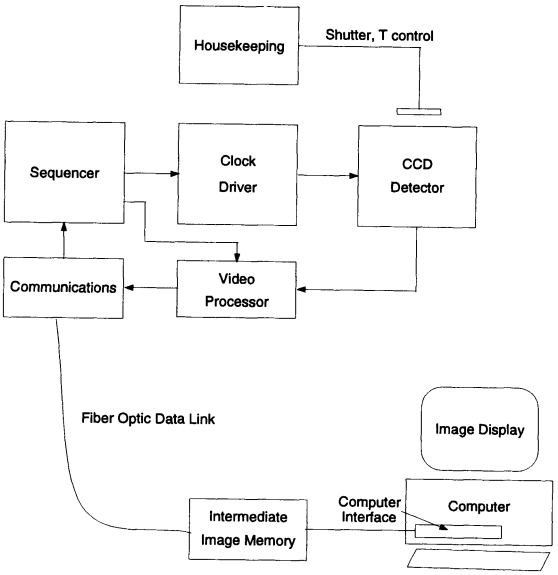

Fig. 1. Block Diagram of a Typical CCD Controller

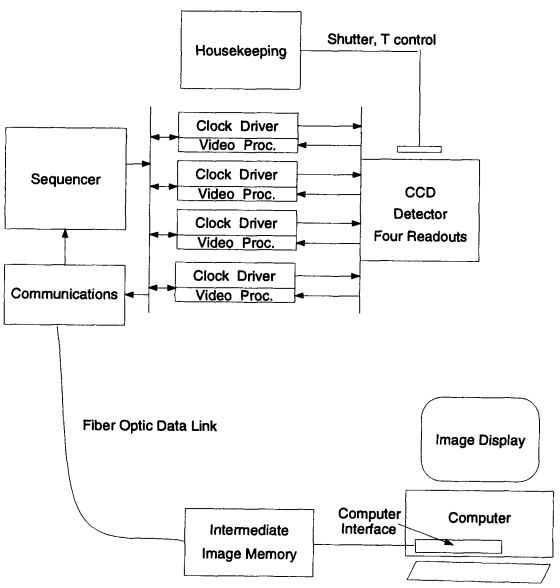

Fig. 2. Block Diagram of a Four-Readout CCD Controller

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3. SAN DIEGO STATE CONTROLLER

In the interests of specificity, the controller design developed at San Diego State University is described. Table 2 shows a listing of some of its characteristics, listing both the current controller that has been in extensive use, and a planned upgrade.

The current controller has a typical readout time of 21 microseconds per pixel, which includes eight microseconds for sampling the baseline after reset, and eight microseconds for sampling the signal after dumping charge on the output node of the CCD. Both voltages are sampled with an analog integrator in the video processor, and their difference is taken also by the integrator by reversing the polarity of its input between the two integrations. An additional five microseconds is used for clocking the serial charge, resetting the output node and transmitting the 16-bit image data over the fiber optic link. The A/D conversion overlaps with the signal integration. An additional overhead of approximately two microseconds is imposed for each additional readout for updating each set of serial shift register clocks and for the fiber optic data transmission since these operations don't take place simultaneously in the current implementation. If the baseline and signal integration times are each reduced to four microseconds then a faster readout can be had at the expense of larger readout noise, and eight readouts can be accomplished in a time of 26 microseconds. The lowest readout noise obtained with these controllers is reported in this conference as 2.0 electrons rms with four + four microseconds of signal processing time. The system noise is estimated by measuring the rms noise with the input to the video processor grounded at 0.7 A/D units. Most of this is contributed by the A/D converter (0.55 ADU) with the rest evenly divided amongst the video processor stages. At typical system gains this figure corresponds to 1-3 electrons rms readout noise and is not a significant noise source.

The board size is 10 x 26 mm, which is the 3U VME width and a fairly long length. Power dissipation for two readouts is 23 watts, with much of it produced by the analog circuits. Three circuit boards are required for implementing one readout, and one board is required for each additional readout. The practical maximum number of readouts is about eight, with the limit placed by issues such as system size, power dissipation, readout speed inefficiencies and cost. More readouts can be implemented since the digital addressing and backplane transmission accommodates up to 32 readouts, but it becomes a relatively unsuitable system architecture with so many readouts.

The only computer interface currently supported is to VMEbus, although users have developed S-bus, Macintosh and NeXT interfaces as well. The A/D converter is a 16-bit, 10 microsecond conversion time monolithic CMOS device. There are two analog gains software selectable in the video processor. The timing sequencer is based on a Motorola DSP56001 monolithic digital signal processor operating at 100 nanoseconds per instruction, which is also the rate at which timing signals can be generated. A wait mode allows timing resolution down to 50 nanoseconds. There are twelve CCD clock drivers operating over a range of ± 10 volts in programmable steps of 0.1 volts.

A planned upgrade to the controllers focuses around improving the readout speed and the efficiency of supporting a large number of readouts. There are three motivations for improving the readout speed, as follows: (a) Current systems are often used at the telescope or in development labs to acquire images either at high illumination levels or in setup modes where

TABLE 2

San Diego State controller parameters for N readouts

	Current	Planned
Typical readout time	(21 + 2 x N) μsec/pixel	18 μsec/pixel
Fastest readout time for N = 8 readouts	26 μsec	3.2 μsec
Readout noise	0.7 ADU system noise 2.0 e^- with LL CCD (Luppino)	
Board size	10 x 26 mm	10 x 23 mm
Power dissipation for 2 readouts	23 watts	18 watts
Boards needed for four readouts	6	4
Practical maximum number of readouts N	N = 8	N = 16
Computer interfaces	VME	VME, S-bus
A/D converter	16-bits, 10 μsec/pixel	16-bits, 2μsec/pixel 19-bit w/ auto-scaling
Selectable gain	2 choices	4 choices
Timing sequencer	DSP56001, 100 nsec/instr.	56005, 40 nsec/instr.
CCD clock drivers	12, in 0.1 volt steps	14, in 0.01 V steps

the readout time for large arrays is burdensome. Such operations as focussing, flat field acquisition, lamp calibrations, field identification, and laboratory optimization and characterization often must be done either quickly or many times, where a reduction in readout time by a factor of five to ten with a corresponding increase in readout noise by a factor of two to three is desirable. Current systems cannot accommodate this. (b) Luppino's (1995) result of obtaining two electrons rms readout noise at eight microseconds total signal processing time suggests that future CCDs can have it both ways - very low readout noise at moderately fast readout speeds. Future controllers will need to read from multiple readouts in times shorter than ten microseconds per pixel to exploit this capability. (c) Infrared arrays, although not specifically targeted by current CCD controllers, have been operated successfully with them by several groups. With infrared arrays becoming larger, incorporating multiple readouts to keep their readout time manageable, and having similar readout requirements as the fast mode being discussed here it becomes feasible to have one controller designed for both optical CCDs and infrared arrays. This can reduce the design and maintenance costs at observatories that operate both types of arrays. Of course, it is a challenge to design controllers that don't compromise too much performance in achieving such versatility.

Features of the upgraded design to accomplish faster and more efficient multiple readout

operation are shown in Table 2 in the planned column with the bold items. Faster DSP and A/D converters will be used in an architecture that does not impose a readout time penalty for adding readouts. This will be done by implementing the newer Motorola DSP56005 at a clock speed of 50 MHz and an instruction time of 40 nanoseconds together with hybrid A/D converters with two microsecond conversion times. The clock driver circuit will be changed to the more conventional switched DC arrangement to allow simultaneously updating the clocks going to different CCDs. Surface mount circuit board manufacturing will increase the practical maximum number of readouts to 16 or so by incorporating more than one readout per circuit board.

Other upgrades will be implemented in this process. The clock voltages and DC bias supplies will be specifiable to 0.01 volts rather than 0.1 volts to improve the dispersion from board to board. A 19-bit auto-scaling mode will be implemented to handle large dynamic range readouts as was discussed above. More choices of video processor gain will be provided. A mode to DC couple the video processor to the array readout will be provided for operating infrared arrays. An S-bus computer interface will be implemented to allow direct connection to compact Sun workstations. Expanded memory will be provided by the internal program memory space of the DSP56005 (4608 words) and by external X: and Y: data memory (32k words total). An in-circuit emulator feature of the DSP56005 will be accessible by connection to Motorola supported emulator hardware and software to help users diagnose their DSP code. More attention will be paid to power dissipation issues to offset the increased power consumption of the faster A/D converters.

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DISCUSSION

GLASS: Why do you have the image stored between the controller and the computer?

LEACH: To insure that no image data are lost when the computer is a UNIX machine, which has a poor real-time response.

WEAVER: Do you have any problems keeping the DSP clocking noise out of the signal processor chain signal?

LEACH: No. Synchronizing all readout processes is needed.

STOVER: Will your new system have a DSP which is highly synchronized to the readout activity?

LEACH: Yes

STOVER: Will the new generation analog board provide a unique board ID which can be ready by the DSP?

LEACH: It will not be needed because the new analog boards will not need a voltage calibration.

FLORENTIN-NIELSON: Do you find that when performing partial image readout, that the bias will be different from that of a full frame readout?

LEACH: Yes, because the CCD is AC coupled to the video processor.