a multidisciplinary group from the University of Hong Kong has used this method to fabricate efficient PV devices.

W.K. Chan and co-workers used poly(*p*-phenylene vinylene) (PPV) functionalized with ruthenium terpyridine complexes as the photosensitizer for these devices. Sulfonated polyaniline (SPAN) served as the hole-transport material. Each device was fabricated by sequentially dipping an indium tin oxide glass slide into solutions of SPAN and ruthenium-functionalized PPV. After depositing a defined number of SPAN-PPV bilayers, the researchers coated the thin film with a 40 nm aluminum electrode layer.

Thin films made up of 13, 20, and 30 bilayers were fabricated and found to have overall thicknesses of 110 nm, 150 nm, and 190 nm, respectively. The researchers controlled the device thickness by varying the dipping conditions. They measured current–voltage characteristics for all three devices, in the dark and under optical illumination. The maximum short-circuit current and open-circuit voltage were both exhibited by the device comprising 13 bilayers. The team said that although this device has lower absorbance than those with more bilayers, its performance may be due to a lower serial resistance. The external quantum efficiency of the devices was measured and found to agree well with the absorption spectrum of the device. For the device with 13 bilayers, the maximum efficiency was 2.2%, while the device with 30 bilayers showed an efficiency of 5%. This maximum efficiency occurs at an optical wavelength of ~510 nm, in agreement with the maximum absorption of the ruthenium dye. The researchers conclude that the enhancement of the efficiency is due to the presence of the metal sensitizers.

The researchers propose that by working with a mixture of metal complexes with varying absorbance maxima, it may be possible to use electrostatic self-assembly to prepare detectors with photosensitivity over a wide range.

CATHERINE OERTEL

Simulations Show Formation of Inorganic Nanotubes within SWNTs

Low-dimensional inorganic crystalline structures analogous to single-walled carbon nanotubes (SWNTs), called ionic inorganic nanotubes (IINTs), have been prepared with both physical and chemical methods. The structure of IINTs formed by filling SWNTs with molten salts can be related to crystalline sheets, just as SWNTs are related to graphene sheets. Computer models have been employed to determine the stabilities of IINTs but heretofore have not been used to identify new IINT structures worthy of experimental investigation. Recently, however, M. Wilson at the Department of Chemistry, University College London, used atomistic computer models to simulate the formation of a range of novel IINTs by filling SWNTs with bulk inorganic liquids.

In an article published in the February issue of *Nano Letters*, Wilson, a Royal Society Research Fellow, described the controlled formation of IINTs within SWNTs using a relatively simple atomistic computer model. Effective pair potentials control the short-range ion–ion and ion–carbon interactions. With polarization effects also accounted for and parameters chosen to reflect a tetrahedral ion coordination environment, a typical bulk crystal ground state results. The SWNTs, formed by folding single graphene sheets, were treated as fixed atomistic tubes. Molecular dynamics simulation techniques were applied to fill the SWNTs with bulk molten ions and to form the IINTs. Molecular mechanics geometry optimizations were then used to produce an effective IINT formation phase diagram, which shows that the dominant factor controlling IINT morphology is the SWNT diameter. For example, both (5,2) and (4,3) IINTs, whose diameters are 7.29 Å and 7.10 Å, respectively, form within (19,0) or (11,11) SWNTs, whose diameters are 14.90 Å and

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14.94 Å, respectively. Here, the integers in parentheses (*n*,*m*) allow a topographical characterization of the chirality of the nanotube in comparison with the lattice vectors that span the graphite lattice. Wilson deems the fact that IINTs with very similar diameters but different morphologies can form in the same SWNT as indicative of significant kinetic control of IINT morphology. Wilson said that his simulations show "that a class of IINT structures, analogous to those formed by elemental carbon itself, may exist and that an experimental pathway to such structures may lie in the filling of [SWNTs] from the liquid phase."

Two alternate IINT morphologies investigated by Wilson are related to hexagonal or square-net sheets. Energies of geometry-optimized (5,0) IINTs plotted as a function of ion density show double minima, which Wilson attributes to the two morphologies, with the square-net minimum occurring at a higher density than the hexagonal. For (5,2) IINTs formed in small-diameter SWCNTs, the square-net structure is the stable morphology.

Wilson said that the presence of multiple energy minima suggests that a pressure-driven pathway may exist between the square-net and hexagonal IINT morphologies. Indeed, the application of pressure in a simulation of a (14,14) SWNT (diameter, 19.01 Å) filled with bulk molten ions led to the formation of nested, double-walled IINTs—one IINT with morphology (3,2) inside a (9,2) IINT. Wilson said that "this demonstrates that both the [SWCNT] pore diameter and the external pressure have the potential to effectively control both the IINT morphology and the degree of nesting."

STEVEN TROHALAKI

Tungsten Electrodes Reduce Parasitic Source/Drain Resistance of Poly-Si TFT

Polycrystalline silicon thin-film transistors (TFTs) are of potential interest for applications in peripheral circuits for active-matrix liquid-crystal displays, but device dimensions must be scaled down in order to improve speed and circuit densities. In the February issue of *Electrochemical and Solid-State Letters*, H.-W. Zan of the National Chiao Tung University, T.-C. Chang of the National Sun Yat-Sen University, P.T. Liu of the National Nano Device Laboratory, and their colleagues have proposed a method for decreasing parasitic resistance of TFTs by the use of tungsten electrodes.

The research team from Taiwan created TFTs by conventional methods in which a 30 nm a-Si layer is deposited by low-pressure chemical vapor deposition (LPCVD) on oxidized silicon wafers. After active region patterning, a 60 nm tetraethylorthosilicate (TEOS) oxide layer and subsequently a 300 nm a-Si layer were deposited by LPCVD. The a-Si layer was then recrystallized by solid-phase crystallization at 600°C for 24 h. After defining the gate by reactive ion etching (RIE) and removing the oxide on source/drain (S/D) regions by HF dip, a lightly doped drain implant was performed using phosphorus ions at a dose of 3×10^{13} cm^{-2}. Then, a 200 nm oxide side-wall spacer was formed abutting the gate by conformal deposition of a TEOS oxide layer and subsequent RIE. Next, phosphorus ions at a dose of 5×10^{15} cm^{-2} were implanted to form the S/D region. Dopants were activated by a rapid thermal anneal at 750°C for 20 s. After removal of the oxide from the S/D

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