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Five-element Digital Corrector Receiver for the Chinese Spectral Radioheliograph

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Abstract. The design of five-element digital receiver system is decribed. At first, we analyzed the process of data processing in the receiver system. Then we wrote programs to implement the FIR parallel filter and showed its simulation results. Finally the testing result of the correlation receiver system is demonstrated.

Keywords. FIR parallel filter, correlation receiver

1. Introduction

By using the FPGA, the procedure of signal processing can be achieved very flexibly and easily. In this way, a five-element digital receiver system was developed to pretest and calibrate the Chinese Spectral Radioheliograph(Yan *et al.* 2006,2009). It can also be used for other astronomical applications. The FIR parallel filter is an important module in the receiver. Therefore we describe the design of the filter with verilog in detail, and undertake the simulation under appropriate settings.

2. Method and Results

We use CycloneII EP2C50F672 and QuartusII to design the Digital Signal Processing (DSP) unit of digital receiver. There are 5 elements corresponding to 5 channels. Figure 1 shows a block diagram overview of one channel of the DSP(Zhang *et al.* 2006). X(n) is the digitized signal at 1 Gsps (gigasample per second) from IF. Cos(wn) is an agile mixer that converts the input signal into a low frequency. The mixer output, after filtering and sampling, is a narrowband signal with low rate. Then the signal is converted into analyzing signal by Hilbert filter and delay unit. Finally the signal is sent to the correlator to compute with other channels results. The outputs of the correlator are the complex visibility functions.

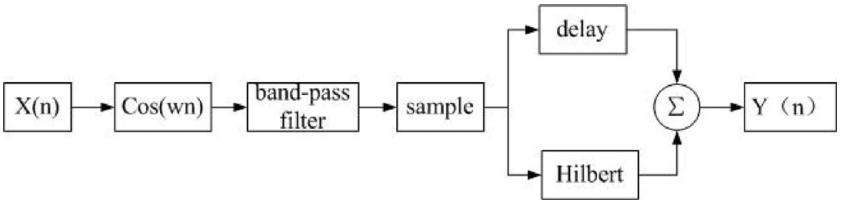

Figure 1. Block diagram of one channel of the five-element digital receiver system.

Although the function of DSP existing in FPGA is tremendous, we need simplified algorithms to reduce the occupancy of FPGA resources. We use 8 parallel filter structure(Zhang *et al.* 2009), CSD coding and bit-plane method. The data rate is reduced

from 1024MHz to 256MHz, largely saving the FPGA resources. We select equiripple algorithm to generate the bandpass filter coefficients by MATLAB. The filter parameters are 127 order, [10,20]MHz, and 41dB stop-band attenuation.

We use the coefficients generated by MATLAB before to build a serial FIR filter and an 8 parallel filter, then input white gaussian noise respectively. The output is shown in figure 2. The left figure is the output of serial filter(dot line) and 8 parallel filter(Asterisk). The right figure is the error between the two filters. The error is as low as 10^{-16}, which indicates that the parallel filter is feasible and efficient.

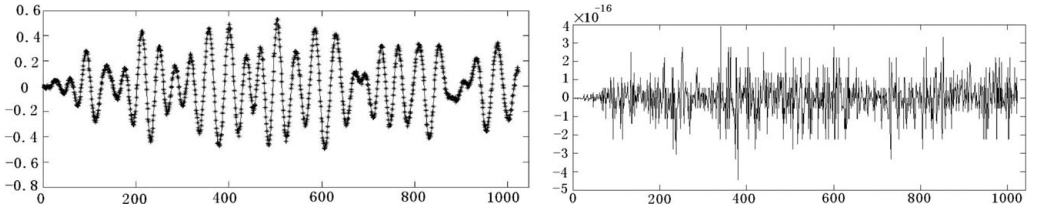

Figure 2. The simulation result of serial filter and parallel filter.

White gaussian noise is input into the receiver. The testing result is shown in figure 3. The correlator value has reached to its maximum at 0ns Delay, which indicates applying the 8 parallel filter to the receiver is feasible and efficient.

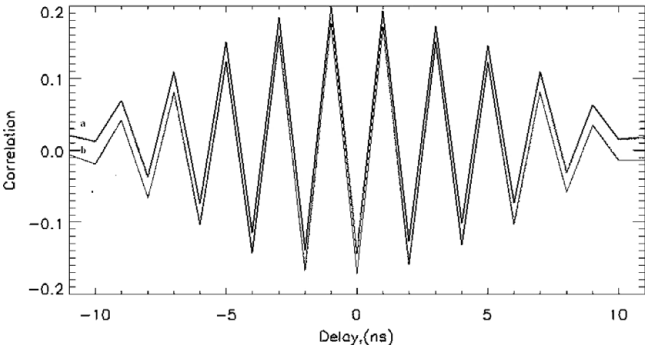

Figure 3. the correlator output with un-quantized data(line a) and quantized data(line b).

3. Conclusion

We use a simplified algorithm to construct 8 parallel filter. By simulating it is confirmed that the algorithm is effective and flexible. We fulfil the DSP algorithm with verilog hardware language. The testing result is consistent with our expection. As a digital subsystem prototype for CSRH, it can provide the opportunity to study the design, calibration, and correlation requirements of CSRH. It also provides the flexibility to process the data with multiple algorithm.

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