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Modern Integrated Circuits: The Ultimate Engineered Material

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From its beginning in the 1960's the semiconductor industry has maintained a relentless pace of innovation and integration, doubling the number of transistors on an integrated circuit approximately every 18 months while at the same time increasing operating speed and performance.

Figure 1 is an SEM cross-section of IC from the early 90's showing a transistor gate, contact and metallization. Most of the salient features of the IC are captured in this one section.

By way of contrast, figure 2 is a SEM micrograph of a modern 45 nm microprocessor showing the astonishing complexity that has been achieved in less than twenty years.

Semiconductors are today a $250B industry and the modern integrated circuit represents the ultimate engineered material. A single centimeter square die can have up to ten levels of wiring running to several kilometers in total length. Minimum horizontal features sizes on the most advanced devices are now 32 nm and controlled to tolerances ten times smaller across wafers measuring 300 mm in diameter. In the vertical dimension, the thicknesses of critical device layers like the gate or capacitor dielectrics are now measured in a few atomic layers.

Transmission Electron Microscopy is one of the few tools available to monitor and verify structural and dimensional tolerance on this scale. It is invaluable for process development, manufacturing and failure analysis of semiconductor devices.

In additional to these dimensional properties, however, there are a host of other properties critical to device performance. Wiring materials need to be of sufficiently low resistance to keep signal delays and power consumption acceptable while also capable of passing increasingly higher current densities without failing. The wiring insulation must not only isolate without breakdown or leakage its dielectric constant needs to be continually lowered to keep parasitic capacitance between wires acceptable.

In the transistor itself, the work function of the gate needs to be properly tuned to provide both high On state current drive and low Off state leakage level. Similar considerations apply to the gate dielectric. It needs to provide high capacitive coupling between gate and channel for proper control but still insulating the two from DC leakage currents.

In memory devices, like Flash or DRAM, the storage cells have become increasingly sophisticated. DRAM cell capacitors are now elaborate there dimensional structures with exotic capacitor dielectrics.

Until fairly recently the semiconductor industry was able to meet most of these requirements by simply scaling. The dimensions of all critical features – wires, transistors, cells shrank by 30% per generation.

In this decade however, scaling alone could no longer deliver the required progress and new materials were incorporated to continue the pace of Moore's Law. The most dramatic changes occurred at the 65 nm node with the introduction of SiGe alloys to increase strain into the channel to boost electron mobility and subsequently at the 45 nm node with the introduction of hi-K dielectrics and metal gates. Once again,

the TEM is one of the few tools available with the necessary spatial resolution and materials sensitivity to allow device engineering and fault diagnosis at this scale and complexity.

This paper will survey the different structures and materials combinations used on modern ICs, give examples of useful TEM and TEM related techniques to measure them and discuss the challenges involved.

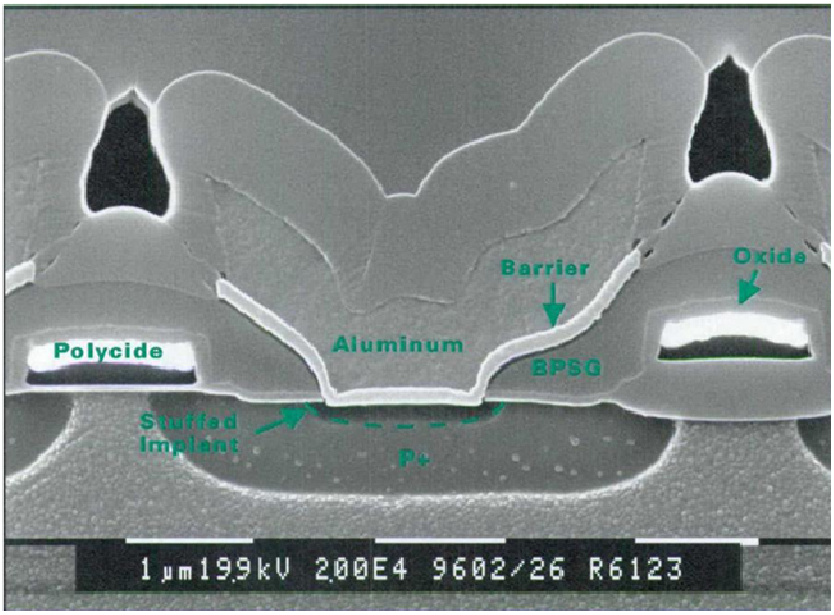

Figure 1: SEM Cross-section of an integrated circuit circa 1991

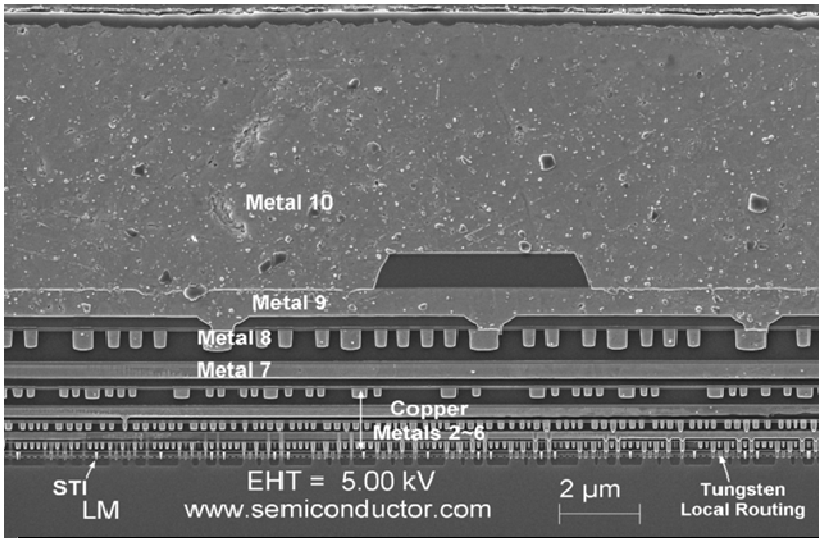

Figure 2: SEM cross-section of an IC circa 2008

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