

3D Analytical TEM Approach to Effectively Characterize 3D-FinFET Device Features in Semiconductor Wafer-foundries

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Introductions of 3-Dimensional FinFET transistors in semiconductor device open a new era for continuous shrinkage of semiconductor transistor nodes. One big challenge for physical failure analysis (PFA) and transmission electron microscopy (TEM) is that, for device of 20nm, 14nm, and beyond, features of interests (FOI) are mostly thinner than a thickness of a TEM lamella (say, around 50~150nm), depending on the orientation. This adds in ambiguity in interpretation of the TEM imaging straightforward. Combined with intrinsic complexity from the 3D-FinFET structures themselves, PFA/TEM teams at wafer-foundries truly have to constantly think out of box for novel approaches to effectively and timely isolate faults and conclusively identify root-causes of yield detractors [1~4].

One novel approach, to accommodate aforementioned complicated PFA / TEM cases on 3D FinFET structures, is to introduce 3D TEM characterization by incorporating several traditional TEM routines, without prolonging turnaround. Basically, there are three steps. Step-I, machine a planar view (top-down) TEM lamella with the FOIs in the central region, by focused ion beam (FIB) lift-out. Most importantly, the TEM lamella has to be kept relatively thick on purpose, to avoid prematurely remove layers with defects. Step-II, employ x-ray energy dispersive spectroscopy (XEDS) elemental mapping in an Analytical TEM to explore and pin-point the abnormality. Step-III, extract another cross-sectional TEM lamella right at the location of the abnormal region in the existing thick planar-view TEM lamella, with desired orientation by FIB lift-out. Thanks to technology development of new XEDS hardware, nowadays, fault-isolations by XEDS mapping can be done in 5~10 minutes, e.g., by a Super-X detector, which eliminated the concerns of turnaround time and potential artefacts due to sample-drifting.

Demonstrated here is one successful example for the effectiveness of this novel best practice of 3D TEM. The PFA case was for a testing device from a wafer processed during a CMP tool-qualification, back to 1st-Si stage of 14XM 3D FinFET technology ramp-up. Figure-1 is a schematic view of 3D FinFET structure. Figure-2a is a planar view TEM image, and Figure-2b displays the corresponding XEDS elemental mapping, with overlay of elements, Ti, Hf, and W. If without the navigation from the top-down view XEDS mapping, the pinching of 1st Fin, and distinctions of Ti-rich / Ti depletion regions could have been easily overlooked or even cut through during the progressive FIB, if only by traditionally cross-sectional TEM all the times. Figure-3 is a FIB image illustrating where the additional cross-sectional TEM lamella was extracted from the first planar-view TEM lamella. Figures 4(a) and 4(b) are TEM, and overlay of HAADF-STEM with XEDS mapping on the cross-sectional TEM lamella, which validated the pinch of the 1st FIN, and revealed over-polishing of the FINs / Gates by the CMP process.

References:

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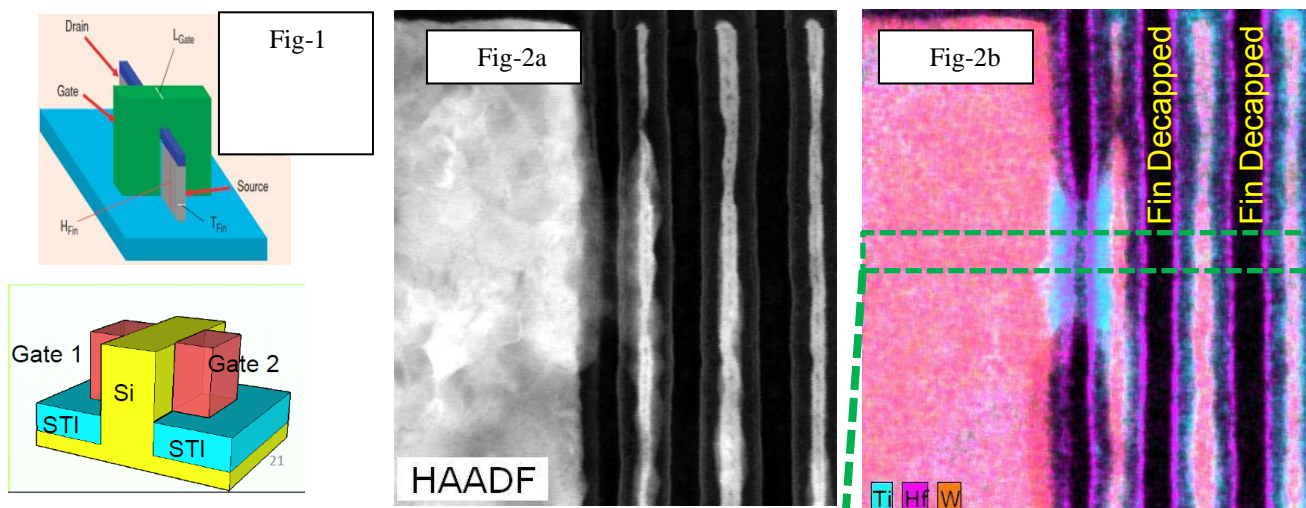


Figure 1. An illustration of 3D FinFET (Courtesy: after Chenming Hu, Aug-2011).

Figure 2. (a) planar-view TEM; and (b) overlay of corresponding XEDS maps of Elements, Ti, Hf, W.

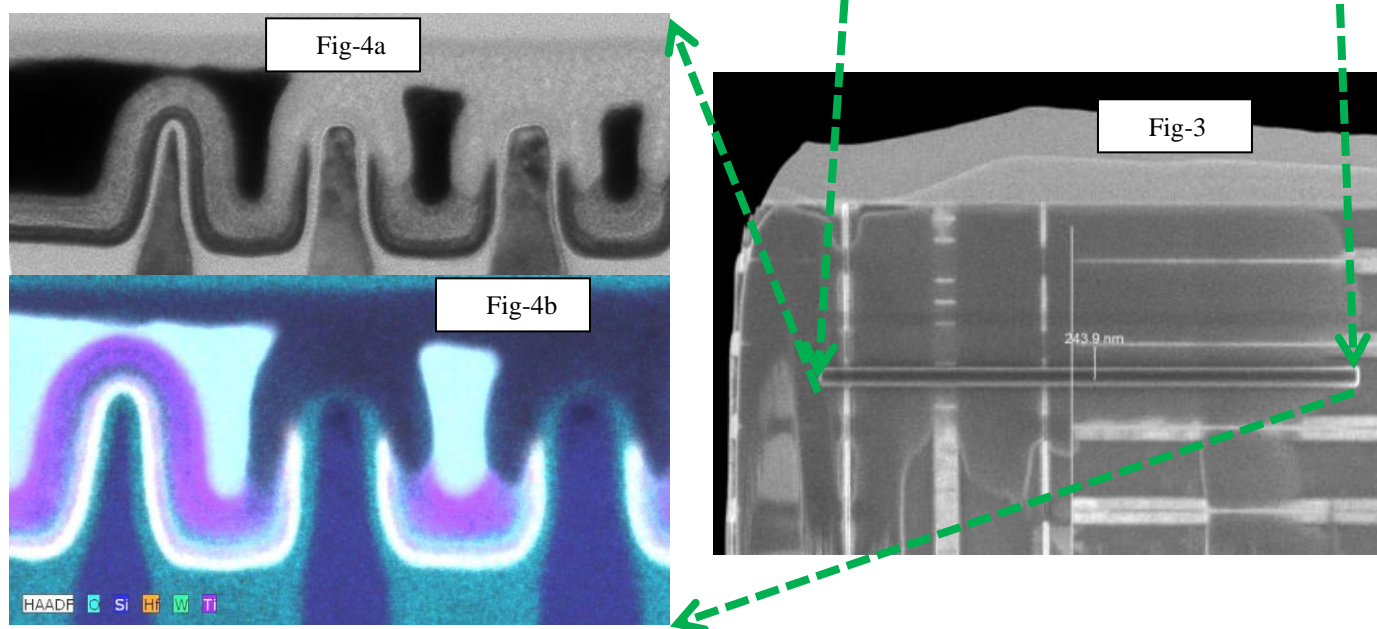


Figure 3. FIB image for the 2nd cross-sectional TEM lamellar on top of the planar TEM lamella being XEDS mapped.

Figure 4. (a) TEM image, and (b) HAADF-STEM image overlay with XEDS elemental maps, from the cross-sectional view TEM lamella.