Supercritical Carbon Dioxide Technology Offers Ecological and Cost-Effective Way to Clean Chips

Four main methods are available to produce a specific chip—layering, patterning, doping, and heat treatment. In patterning and doping, a polymeric coating is applied to the surface of a silicon wafer, and the coating is patterned using photolithography, in which a high-intensity light exposes a pattern into the polymeric photoresist. The photoresist will either become a shorter chained (weaker) polymer or a cross-linked (stronger) polymer in the exposed region, depending on the type of resist. The weaker polymer is chemically dissolved. The remaining photoresist is then removed by using radio-frequency plasmas in an "ashing" step, followed by a wet-chemistry solvent rinse with aggressive acids and/or corrosives or organic chemicals. However, since feature sizes of 130 nm will be making entry into the market by the fourth quarter of 2001, and smaller dimensions are on the way with higher aspect ratios (10:1, in some cases), traditional wet chemistry stripping will become less successful at cleaning the wafers. Surface tension and capillary forces of the liquids will not allow penetration into the deep, high-aspect-ratio features on the chip (if wetting is not obtained).

While chip-making is referred to as a "clean industry," on an average day of operations at a wafer-fabrication plant, an estimated four million gallons of wastewater and thousands of gallons of corrosive hazardous materials, such as hydrochloric and sulfuric acids, are produced during the cleaning process.

An innovative technology called SCORR (supercritical carbon dioxide resist removal) has been developed at Los Alamos National Laboratory (LANL) as a cleaner approach to photoresist removal. By pressurizing and heating liquid carbon dioxide above its critical pressure and temperature (~7450 kPa and 32°C) it becomes a supercritical fluid. The supercritical carbon dioxide ($scCO_2$) exhibits gaslike viscosity and liquidlike density, with diffusivity between that of a gas and a liquid, but with no surface tension. It replaces the hazardous chemicals used to strip the photoresist from the silicon wafer. In addition to the solvent replacement, millions of gallons of ultrapure water used to rinse away the solvents are no longer needed. When the pressure and temperature are lowered, the $scCO_2$ returns to the gas phase, leaving the wafer completely dry and with no residue. This eliminates the need for an isopropyl alcohol drying step that follows the conventional ultrapure water-rinse step.

By itself, $scCO_2$ is ineffective at photoresist removal, so it is generally combined with small amounts of other solvents. The co-solvents used in the SCORR process (such as propylene carbonate) are much safer than the typical methyl ethyl ketones (MEKs) used currently in industry. The defining step of the SCORR process involves swelling of the polymeric photoresist by the carbon dioxide. After swelling, $scCO_2$ creates stresses at the wafer-resist interface. The swelling allows the co-solvent to penetrate into the interface and break the bonds, releasing the photoresist. The photoresist is not solubilized in the $scCO_2$, but is completely debonded from the substrate. Subsequent pulses of $scCO_2$/co-solvent wash the photoresist away, leaving the wafer completely clean and eliminating the need for plasma etching or solvent/alcohol rinsing.

The process is designed as a closed-loop system. The CO_2/co-solvent/polymer mixture is transferred to a separation/filtration vessel, where the detached photoresist is easily removed from the fluid by filtering the mixture. The added co-solvents are then separated from the $scCO_2$ by lowering the temperature and pressure, thereby returning the CO_2 to a gas phase. The co-solvents are collected and can be recycled.

The researchers have removed photoresists and sidewall residues left from etch/ash processes, and have removed Novalac-based resins, poly (methyl methacrylate) (PMMA), deep-UV, and other photoresists on silicon, silicon dioxide, and low-*k* dielectric materials, without modifying the underlying substrates or previously created layers. They have also removed photoresists and sidewall post-etch/post-ash residues left after the single- and dual-damascene processes. SCORR is highly effective on photoresist and resist residue from ion-implantation steps at any dose level. In Figure 1, the vias are shown as received (Figure 1a) and as cleaned by the SCORR process (Figure 1b).

Carbon dioxide is inexpensive, nonflammable, nontoxic, recyclable (in small amounts), and plentiful. In addition, high-purity co-solvents are readily available. Elimination of the rinsing and drying steps of the wafer-cleaning process reduces the amount of energy, water, and time required for processing. The SCORR process can help the semiconductor industry comply with federal and state environmental regulations because the process greatly reduces hazardous wastes and emissions. The co-solvents used are cheaper and safer than the solvents and chemicals currently used, making this an efficient, inexpensive, environmentally safe, and enabling technology.

Although specifically developed to remove even hard-baked photoresists and residue from semiconductor wafers without damaging underlying materials, the SCORR system can be used in any manufacturing process requiring photoresist masking, such as printing, ion

Technology Advances provides up-to-date reports of materials developments that show potential to bridge the gap between research innovation and application of advanced materials technologies. If you encounter or are involved with materials research that shows potential for commercialization and would like to present these developments, contact Renée G. Ford, Renford Communications, Ltd., P.O. Box 72, Harrison, NY 10528-0072; tel. 914-967-0955; fax 914-967-7927; or e-mail renford@compuserve.com.

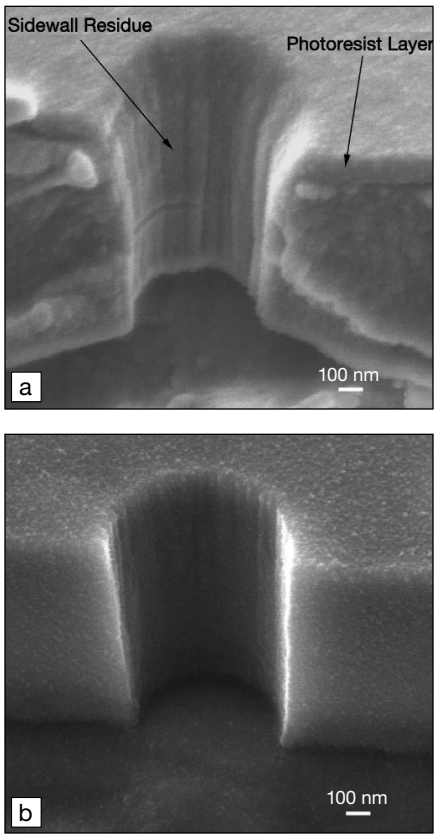

Figure 1. Representative post-etch/post-ash semiconductor via (a) before and (b) after cleaning using the SCORR (supercritical carbon dioxide resist removal) process.

https://doi.org/10.1557/mrs2001.170 Published online by Cambridge University Press

implantation, etching, or the production of optical waveguides. Other potential applications include flat-panel displays, microelectromechanical systems, nanofabrication, precision cleaning, polymer chemistry, interfacial chemistry, materials process compatibility, coating removal, and general coating deposition.

Opportunities

The LANL researchers invite industrial and academic interactions, from basic research collaborations to joint application research and development.

Source: For the Technology: A. Michael Peters or Gunilla Jacobson, Applied Chemical Technology Group, PO Box 1663, MS E537, Los Alamos National Laboratory, Los Alamos, NM 87545, USA; tel. 505-667-3781, fax 505-667-6561, and e-mail ampeters@lanl.gov or jacobson@lanl.gov; URL www.scrub.lanl.gov. *For Technology Transfer:* Randy Tremper, Industrial Business Development Office; tel. 505-665-2134, fax 505-665-3135, and e-mail rtremper@lanl.gov.

Thin Monocrystalline Silicon Films on Flexible Substrates Enable Multiple Transfer Processes

The Institute of Physical Electronics (*ipe*) at the University of Stuttgart, Germany, has developed a process that allows the transfer of epitaxially deposited monocrystalline silicon thin films of high electronic quality from a host wafer to a foreign substrate. This process, which eliminates the need for wafer thinning, also enables multiple transfer processes using a single silicon wafer.

The epitaxial silicon film is grown on top of a monocrystalline silicon wafer that has been treated to allow the subsequent separation of the film. The treatment of the wafer, which consists of anodic etching in a hydrogen-fluoride-containing solution, is a two-step process during which an etching current is switched from low to high current density. This process results in a layered structure that is composed of a dense, 1–2-µm-thick porous layer on top of a submicron-thin, buried, porous layer with lower density. When the wafer is heated to a high temperature of around 1100°C, both of these porous layers recrystallize. This treatment forms a monocrystalline layer on top that contains submicron-sized voids, which is referred to as quasi-monocrystalline silicon (QMS). The buried layer that previously had a high porosity contains only very little silicon after recrystallization. The layer is therefore mechanically weak and enables the detachment of the QMS layer from the original wafer.

During recrystallization, the pores near the surface of the QMS film close. Therefore, an undisturbed surface is obtained that enables epitaxial growth. This technique allows multiple use of a silicon wafer for epitaxial growth by repeated separation-layer formation, epitaxy, and detachment of the epitaxial film. While still attached to the host wafer, the layer can undergo processing steps including wet etching as well as high-temperature processing. After device fabrication, the layer is detached from the wafer and transferred to a foreign substrate.

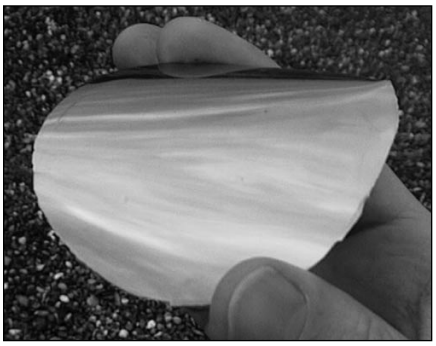

Figure 1. A flexible, monocrystalline epitaxial film, 15-µm thick with a diameter of around 7.5 cm, which was grown on a silicon wafer with a diameter of 10 cm using the quasi-monocrystalline (QMS) process (anodic etching of the wafer, recrystallization, and epitaxial growth followed by detachment of the layer). After growth, it was transferred to a 250-µm-thick, flexible, transparent plastic foil.

The *ipe* researchers have demonstrated the transfer of a 15-µm-thick epitaxial film from a 1.5-µm-thick QMS film to plastic foils. As shown in Figure 1, these films are flexible even though monocrystalline. Investigation of the electronic quality of the epitaxial layers shows that the diffusion length is in the range of 100 µm, which demonstrates the high electronic quality of this material. Potential applications for this technique are wearable microelectronic devices and applications that require flexible electronics. In photovoltaics, *ipe* has achieved thin-film solar cells, using a 45-µm thick monocrystalline Si film transferred to glass, with an efficiency of 16.6%.

Opportunities

The Institute of Physical Electronics is interested in establishing industrial collaborations for display, photovoltaic, and microelectronic applications.

Source: C. Berge, Dr. R. Bergmann, and Prof. Dr. J. Werner, Institute of Physical Electronics, Pfaffenwaldring 47, D-70569 Stuttgart, Germany; tel. 49-711-685-7141, fax 49-711-685-7143, and e-mail juergen.werner@ipe.uni-stuttgart.de; URL www. ipe.uni-stuttgart.de.

Semiconducting Oxides Prepared in the Form of Nanobelts

Binary semiconducting oxides, such as zinc oxide (ZnO), tin oxide (SnO_2), indium oxide (In_2O_3), and cadmium oxide (CdO), are widely used as transparent conducting oxide (TCO) materials [see theme in *MRS Bulletin* **25** (8) (2000) p. 15] and gas sensors. For example, fluorine-doped SnO_2 films are widely used in architectural glass applications because of their low emissivity for thermal infrared heat; SnO_2 nanoparticles are regarded as an important sensor material for detecting leakage of several inflammable gases, owing to their high sensitivity to low gas concentrations; and ZnO is considered an alternative material for indium tin oxide (ITO) in future display applications because of its lower cost and easier etchability than traditionally used materials. These oxides are prepared largely in the form of powders, dispersed particles, or condensed films. Recently, quasi-one-dimensional semiconducting-oxide nanostructures that have a rectangular cross section, corresponding to a belt-like (or ribbonlike) morphology, have been synthesized by researchers at the Georgia Institute of Technology (Georgia Tech).

Their process for producing these "nanobelts" involves the thermal evaporation of oxide powders under controlled conditions without the presence of a catalyst. Commercially obtained oxide powders are placed at the center of an alumina (Al_2O_3) tube that is inserted in a horizontal tube furnace, and the temperature, pressure, and evaporation time are controlled. Long nanobelts have been synthesized of ZnO, SnO_2, In_2O_3, CdO, gallium oxide (Ga_2O_3), and lead oxide (PbO_2) by evaporating the desired commercial metal-oxide powders at high temperatures. The researchers expect that the same technique can be used to fabricate more complex oxides.

https://doi.org/10.1557/mrs2001.170 Published online by Cambridge University Press

The as-synthesized oxide nanobelts are pure, structurally uniform, and single-crystalline, and most are dislocation-free. The rectangular cross sections have typical average widths of ~200 nm, width-to-thickness ratios of 5:10, and lengths of up to a few millimeters. Figure 1a shows a scanning electron microscopy image of as-synthesized SnO_2 nanobelts. Figure 1b, the corresponding transmission electron microscopy (TEM) image, shows their uniform size and size distribution. In Figure 1c, the cross-sectional TEM image of a nanobelt shows its rectangular shape and typical thickness. Each nanobelt is a dislocation-free single crystal. The growth direction and surface planes are well defined, and the surfaces are clean and atomically flat. Compared with conventional bulk ceramics, nanobelts are highly flexible and can be bent >90° without breaking.

In addition to the nanobelt structure, some oxides such as CdO and Ga_2O_3 are produced in the form of single-crystal sheets with sizes of the order of several micrometers to several tens of micrometers. Due to the crystal structure of the CdO nanobelts, they can be cut to a desired length by a focused electron or ion beam. This is advantageous for designing and creating one-dimensional nanobelts with specific lengths for nanodevice applications.

The beltlike morphology appears to be a unique and common structural characteristic for the family of semiconducting oxides having cations with different valence states that form materials with distinct crystallographic structures. Their structures are well controlled and the belt shape is defined by specific crystallographic planes. Table I summarizes the growth direction and the surface planes for nanobelts made of various semiconductor oxides.

These structures are reminiscent of the highly perfect, high-strength whiskers that were discovered and studied in the early 1960s. The whiskers were mostly fiberlike, rather than sheetlike. Typically they had simple, high-symmetry crystal structures.

The synthesis technique developed by the Georgia Tech researchers is relatively simple and low-cost. It is expected to be cost-effective to scale-up the technique for commercialization. The as-synthesized materials have high purity and generally do not require further purification for most applications.

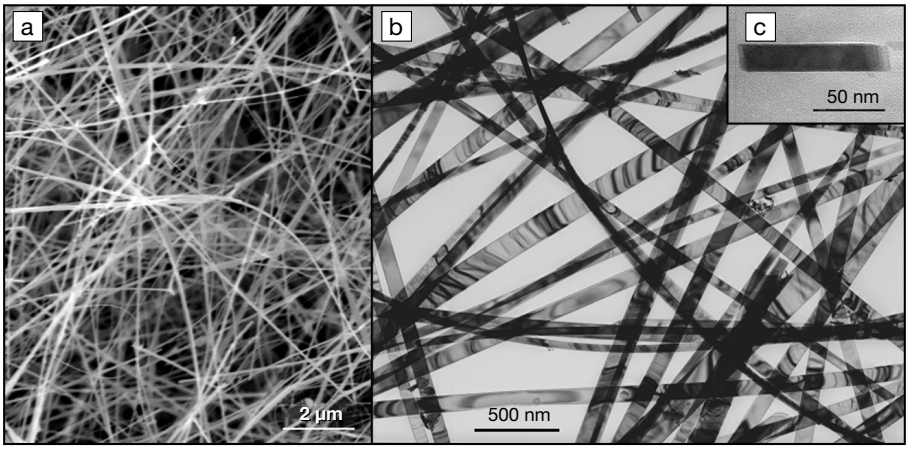

Figure 1. (a) Scanning electron microscopy image of as-synthesized SnO_2 nanobelts. (b) Low-magnification, bright-field transmission electron microscopy (TEM) image, showing the crystalline structure of the nanobelts. (c) Cross-sectional TEM image of a nanobelt, showing its rectangular shape and typical thickness.

Table I: Semiconductive Oxide Nanobelts and Their Growth Directions and Surface Planes.

Nanobelts	Crystal Structure	Growth Direction or Plane	Top Surface	Side Surfaces
ZnO	Wurtzite	[0001]	± $(2\bar{1}\bar{1}0)$	± $(01\bar{1}0)$
ZnO	Wurtzite	[010]	± $(2\bar{1}\bar{1}0)$	± (0001)
Ga_2O_3	Monoclinic	$(10\bar{1})$	± (100)	± (010)
Ga_2O_3	Monoclinic	(010)	± (100)	± $(10\bar{1})$
SnO_2	Rutile	[101]	± $(10\bar{1})$	± (010)
In_2O_3	C-Rare Earth	[001]	± (100)	± (010)
CdO	NaCl	[001]	± (100)	± (010)

Semiconducting oxide nanobelts doped with different elements could be used for fabricating nano-sized sensors because their conductivity changes dramatically when gaseous or liquid molecules attach to their surfaces. They could also be used for fabricating nanoscale electronic and optoelectronic devices because they are semiconductors. Other possible applications include flat-panel displays and smart windows. For example, tin-doped In_2O_3 nanobelts are both highly electrically conductive and optically transparent.

Opportunities

Georgia Institute of Technology is interested in establishing alliances with companies that can aid in the exploration and/or commercialization of this technology.

Source: Prof. Zhong Lin Wang, Director of the Center for Nanoscience and Nanotechnology, School of Materials Science and Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0245, USA; tel. 404-894-8008, fax 404-894-9140, and e-mail zhong.wang@mse.gatech.edu.

https://doi.org/10.1557/mrs2001.170 Published online by Cambridge University Press